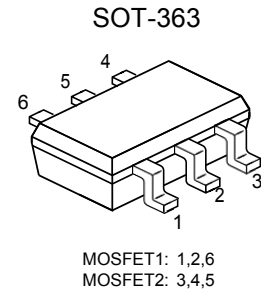


Dual N-Channel Enhancement Mode Field Effect Transistor

FEATURES

- Low on-resistance: $V_{DS}=60V, I_D=300mA, R_{DS(ON)} \leq 1.9 \Omega @ V_{GS}=10V$
- High density cell design for low $R_{DS(ON)}$
- Voltage controlled small signal switch
- High saturation current capability
- Rugged and reliable
- ESD Protection



MECHANICAL DATA

- Case: SOT-363
- Case Material: Molded Plastic. UL flammability
- Classification Rating: 94V-0
- Weight: 0.3 grams (approximate)

MAXIMUM RATINGS $T_A = 25^\circ\text{C}$ unless otherwise noted

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Symbol	Parameter	Rating	Unit	
Common Ratings ($T_A=25^\circ\text{C}$ Unless Otherwise Noted)				
V_{GS}	Gate-Source Voltage	± 12	V	
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	60	V	
T_J	Maximum Junction Temperature	150	$^\circ\text{C}$	
T_{STG}	Storage Temperature Range	-50 to 150	$^\circ\text{C}$	
Mounted on Large Heat Sink				
I_{DM}	Pulse Drain Current Tested①	$T_A = 25^\circ\text{C}$	0.8	A
I_D	Continuous Drain Current	$T_A = 25^\circ\text{C}$	0.3	A
		$T_A = 70^\circ\text{C}$	0.24	
P_D	Maximum Power Dissipation	$T_A = 25^\circ\text{C}$	0.3	W
		$T_A = 70^\circ\text{C}$	0.2	
$R_{\theta JA}$	Thermal Resistance Junction-Ambient	400	$^\circ\text{C/W}$	

Dual N-Channel Enhancement Mode Field Effect Transistor

MOSFET ELECTRICAL CHARACTERISTICS $T_A=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	60	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current($T_A=25^\circ\text{C}$)	$V_{DS}=60V, V_{GS}=0V$	--	--	1	μA
	Zero Gate Voltage Drain Current($T_A=125^\circ\text{C}$)	$V_{DS}=48V, V_{GS}=0V$	--	--	100	μA
I_{GSS}	Gate-Body Leakage Current	$V_{GS}=\pm 12V, V_{DS}=0V$	--	--	± 100	nA
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	1.5	2.5	V
$R_{DS(ON)}$	Drain-Source On-State Resistance ^②	$V_{GS}=10V, I_D=0.3A$	--	1.9	3	Ω
$R_{DS(ON)}$	Drain-Source On-State Resistance ^②	$V_{GS}=4.5V, I_D=0.2A$	--	2.5	4	Ω
Dynamic Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise stated)						
C_{iss}	Input Capacitance	$V_{DS}=30V, V_{GS}=0V,$ $f=1\text{MHz}$	--	12	--	pF
C_{oss}	Output Capacitance		--	3.2	--	pF
C_{rss}	Reverse Transfer Capacitance		--	0.8	--	pF
Q_g	Total Gate Charge	$V_{DS}=30V$ $I_D=0.3A,$ $V_{GS}=10V$	--	0.65	--	nC
Q_{gs}	Gate Source Charge		--	0.12	--	nC
Q_{gd}	Gate Drain Charge		--	0.21	--	nC
Switching Characteristics						
$t_{d(on)}$	Turn on Delay Time	$V_{DD}=30V,$ $I_D=0.3A,$ $R_G=3.3\Omega,$ $V_{GS}=10V$	--	4.5	--	ns
t_r	Turn on Rise Time		--	3.1	--	ns
$t_{d(off)}$	Turn Off Delay Time		-	15	--	ns
t_f	Turn Off Fall Time		--	3.3	--	ns
Source Drain Diode Characteristics						
I_{SD}	Source drain current(Body Diode)	$T_A=25^\circ\text{C}$	--	--	0.2	A
V_{SD}	Forward on voltage ^②	$T_J=25^\circ\text{C}, I_{SD}=0.2A,$ $V_{GS}=0V$	--	0.8	1.2	V

Notes:

① Pulse width limited by maximum allowable junction temperature

② Pulse test ; Pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.

Dual N-Channel Enhancement Mode Field Effect Transistor

Typical Characteristics

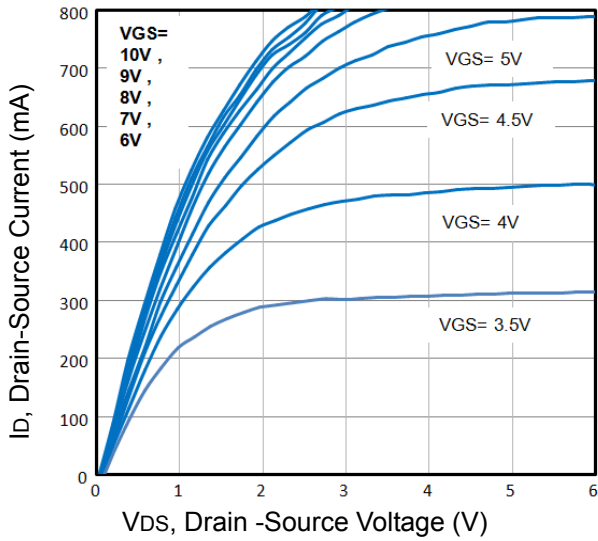


Fig1. Typical Output Characteristics

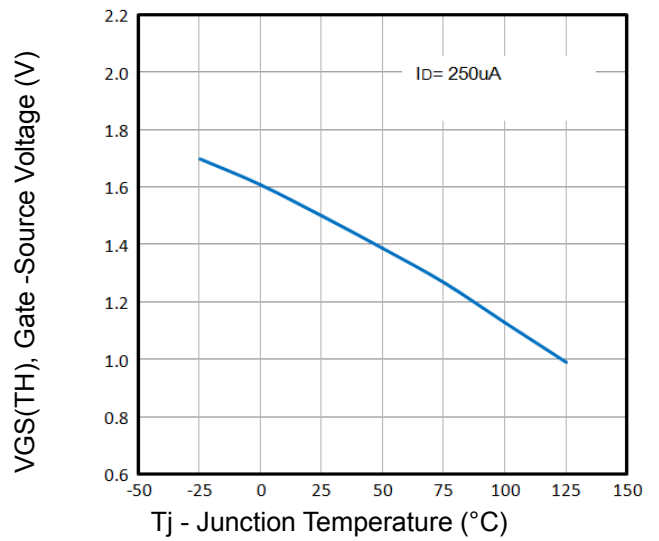


Fig2. Normalized Threshold Voltage Vs. Temperature

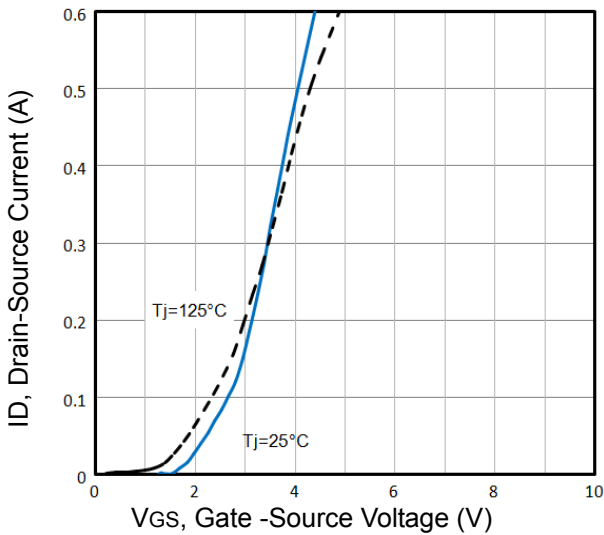


Fig3. Typical Transfer Characteristics

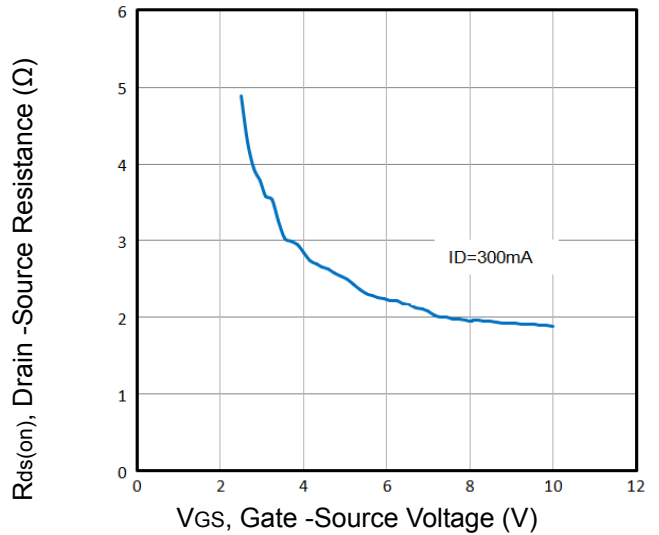


Fig4. Rds(on) vs Gate-Source Voltage

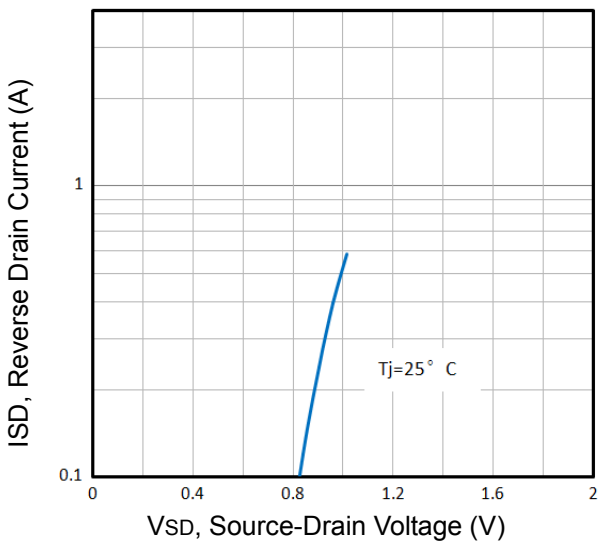


Fig5. Typical Source-Drain Diode Forward Voltage

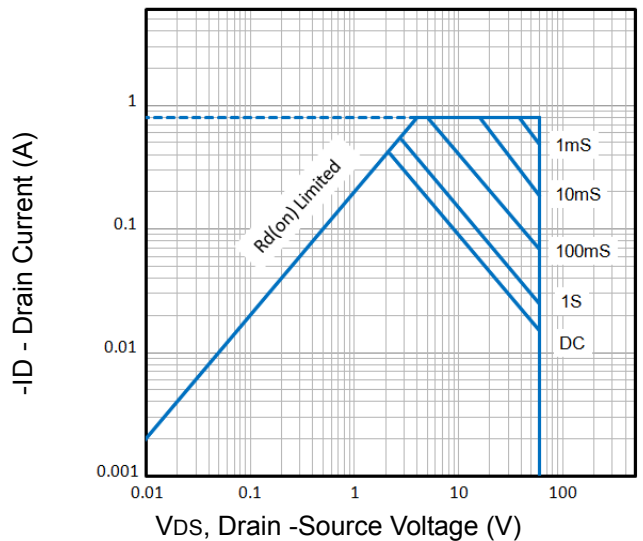


Fig6. Maximum Safe Operating Area

Dual N-Channel Enhancement Mode Field Effect Transistor

Typical Characteristics

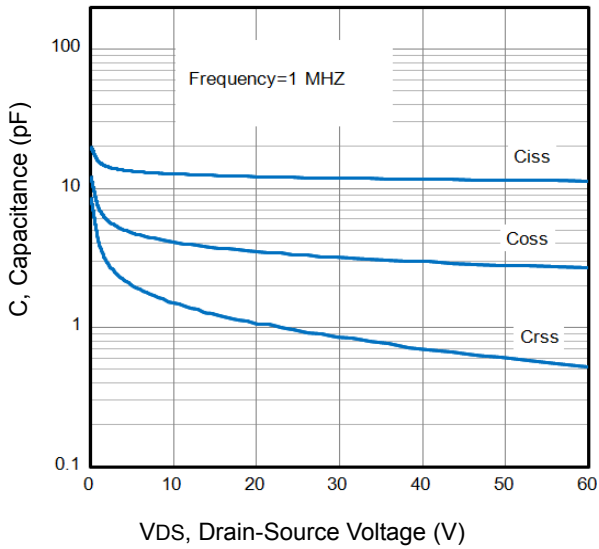


Fig7. Typical Capacitance Vs. Drain-Source Voltage

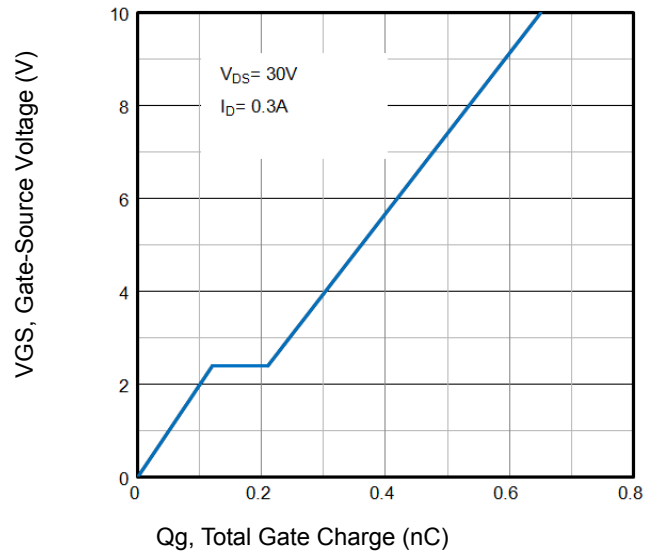


Fig8. Typical Gate Charge Vs. Gate-Source Voltage

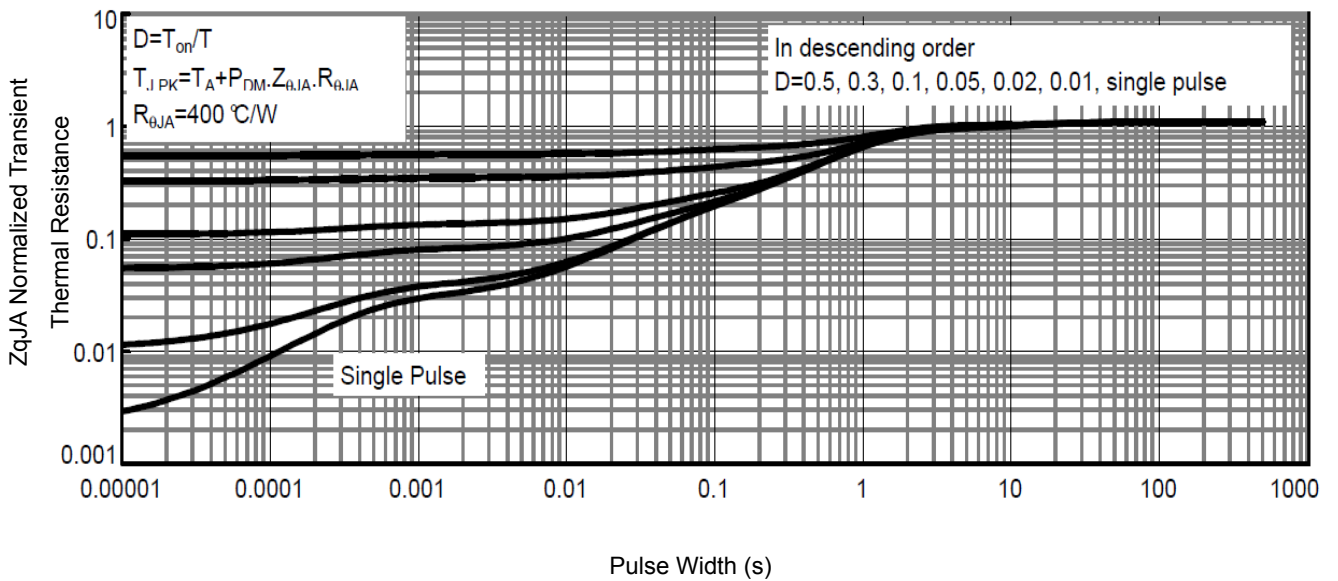


Fig9. Normalized Maximum Transient Thermal Impedance

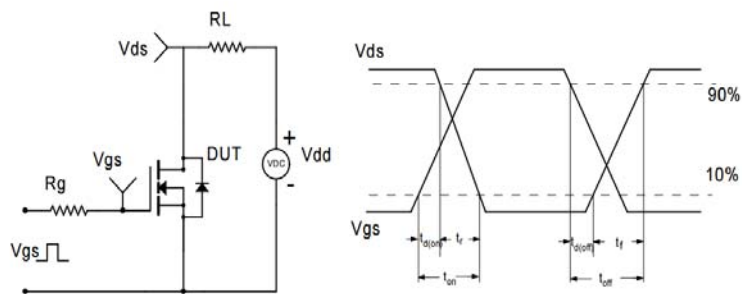
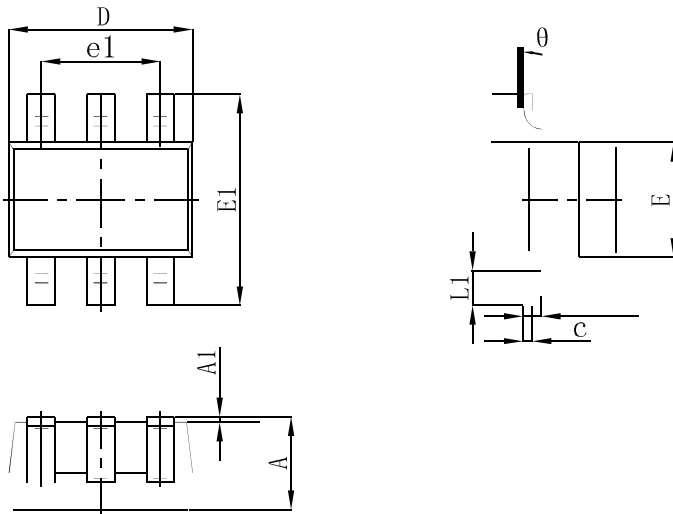


Fig10. Switching Time Test Circuit and waveforms

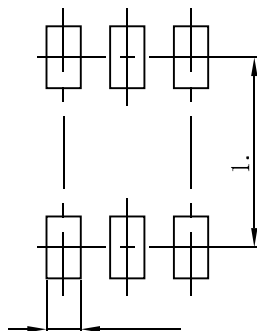
' XDO1 & KDCQH (QKDOFHP HQM RGH) LHG (IIFWUDQMLVRU

627 3DFNDJH2XVQH' LP HQMRQV



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627 6XJJHMMG3DG/ D RXW



' XDO1 &KDGQHQ(QKDGQHP HQM) RGH) LHC(IIFWUDQMLVRU
