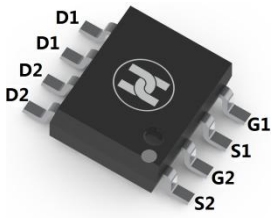
Dual N-Channel Enhancement Mode Field Effect Transistor

FEATURES

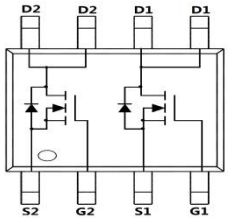
- V_{DS} (V) = 60V
- I_D = 6.3A (V_{GS} = 10V)
- $R_{DS(ON)}$ < 25mΩ (V_{GS} = 10V)
- $R_{DS(ON)}$ < 30mΩ (V_{GS} = 4.5V)



MECHANICAL DATA

- Case: SOP-8
- Case Material: Molded Plastic. UL flammability
- Classification Rating: 94V-0
- Weight: 0.3 grams (approximate)

SOP-8



Absolute Maximum Ratings T_A=25°C unless otherwise noted				
Parameter		**Symbol**	**Maximum**	**Units**
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [A]	T_A=25°C	I_D	6.3	A
	T_A=70°C		5	
Pulsed Drain Current [B]		I_{DM}	40	
Power Dissipation	T_A=25°C	P_D	2	W
	T_A=70°C		1.28	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics					
Parameter		**Symbol**	**Typ**	**Max**	**Units**
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	50	62.5	°C/W
Maximum Junction-to-Ambient [A]	Steady-State		73	110	°C/W
Maximum Junction-to-Lead [C]	Steady-State	$R_{\theta JL}$	31	40	°C/W

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ELECTRICAL CHARACTERISTICS (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250μA, V_{GS}=0V	60			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=48V, V_{GS}=0V			1	μA
		T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±20V			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250μA	1	2.1	3	V
$I_{D(ON)}$	On state drain current	V_{GS}=10V, V_{DS}=5V	40			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=6.3A		20	25	mΩ
		T_J=125°C		34	42	
		V_{GS}=4.5V, I_D=5.7A		22	30	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=6.3A		27		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.74	1	V
I_S	Maximum Body-Diode Continuous Current				3	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=30V, f=1MHz		1920	2300	pF
C_{oss}	Output Capacitance			155		pF
C_{rss}	Reverse Transfer Capacitance			116		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		0.65	0.8	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=30V, I_D=6.3A		47.6	58	nC
Q_g(4.5V)	Total Gate Charge			24.2	30	nC
Q_{gs}	Gate Source Charge			6		nC
Q_{gd}	Gate Drain Charge			14.4		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=30V, R_L=4.7Ω, R_{GEN}=3Ω		7.6		ns
t_r	Turn-On Rise Time			5		ns
$t_{D(off)}$	Turn-Off DelayTime			28.9		ns
t_f	Turn-Off Fall Time			5.5		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=6.3A, dI/dt=100A/μs		33.2	40	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=6.3A, dI/dt=100A/μs		43		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design. The current rating is based on the t≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.

D. The static characteristics in Figures 1 to 6 are obtained using 80μs pulses, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

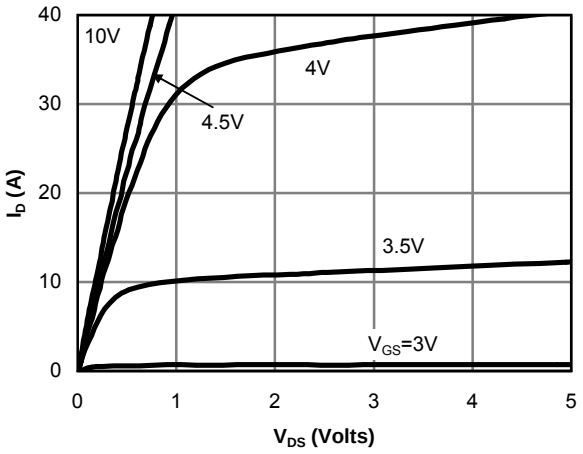

Fig 1: On-Region Characteristics

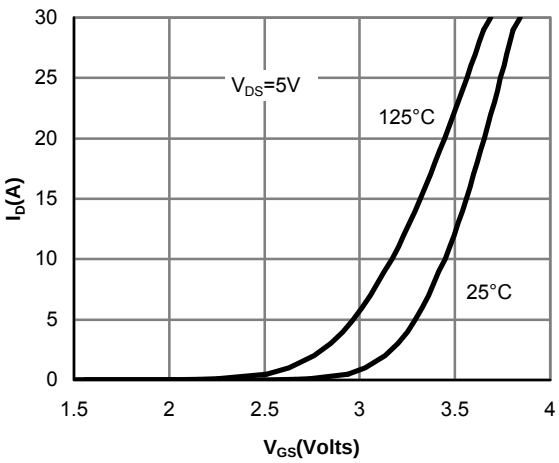

Figure 2: Transfer Characteristics

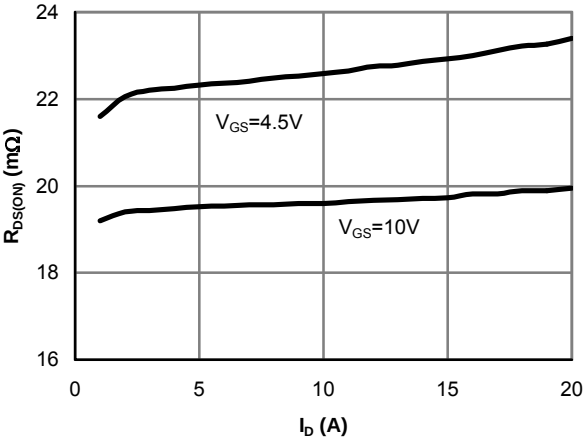

Figure 3: On-Resistance vs. Drain Current and Gate Voltage

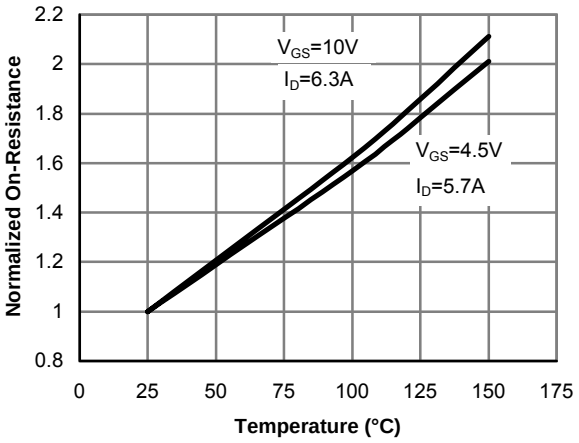

Figure 4: On-Resistance vs. Junction Temperature

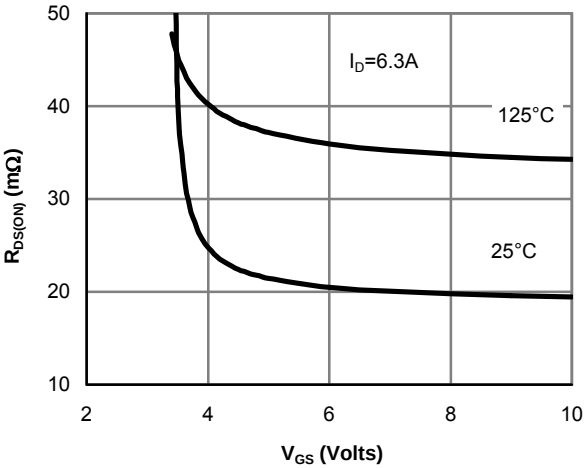

Figure 5: On-Resistance vs. Gate-Source Voltage

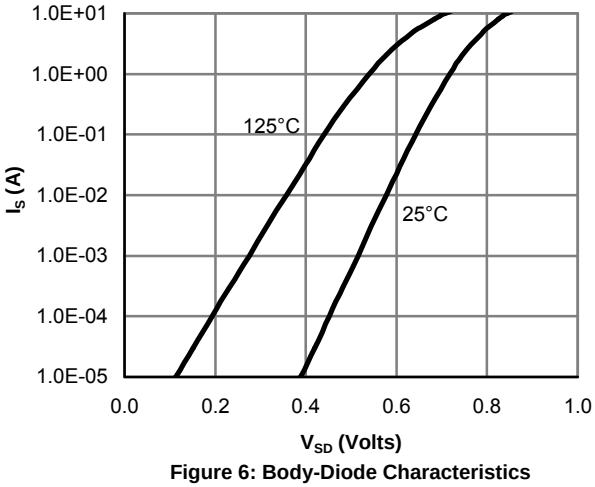

Figure 6: Body-Diode Characteristics

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

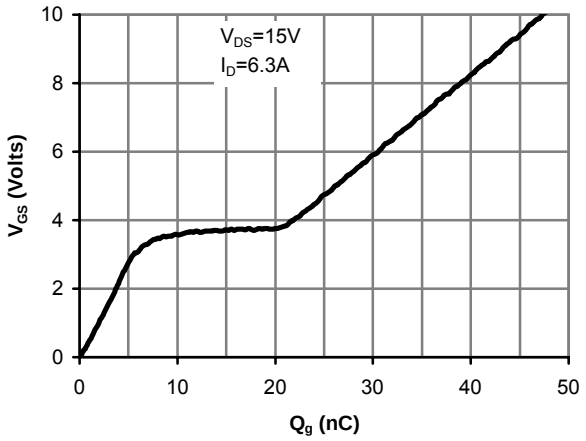

Figure 7: Gate-Charge Characteristics

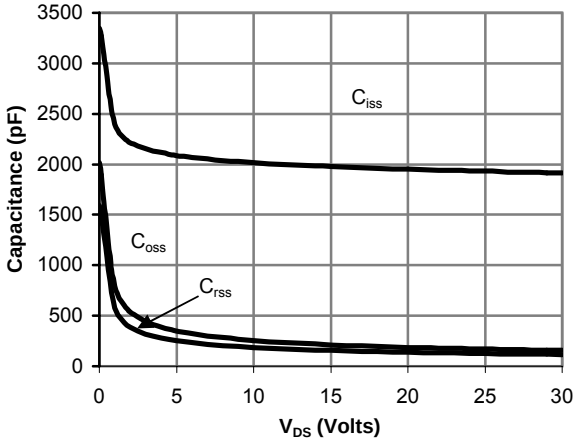

Figure 8: Capacitance Characteristics

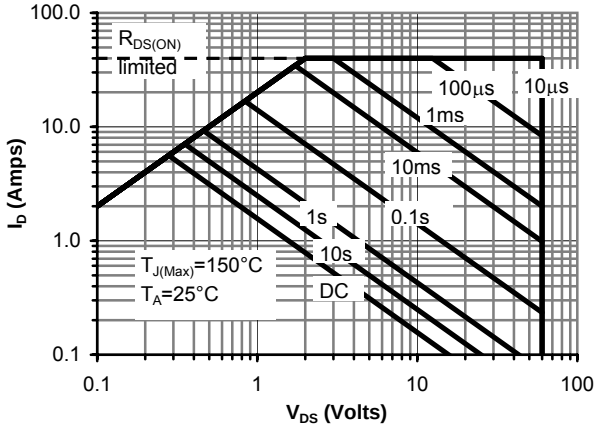

Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

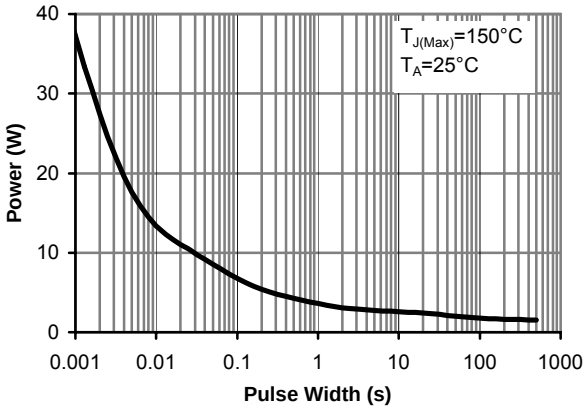

Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

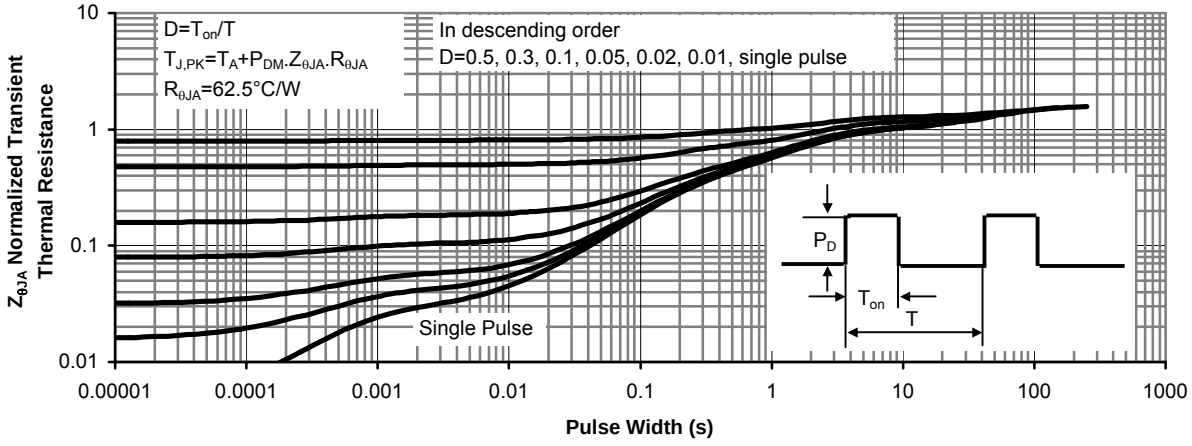

Figure 11: Normalized Maximum Transient Thermal Impedance

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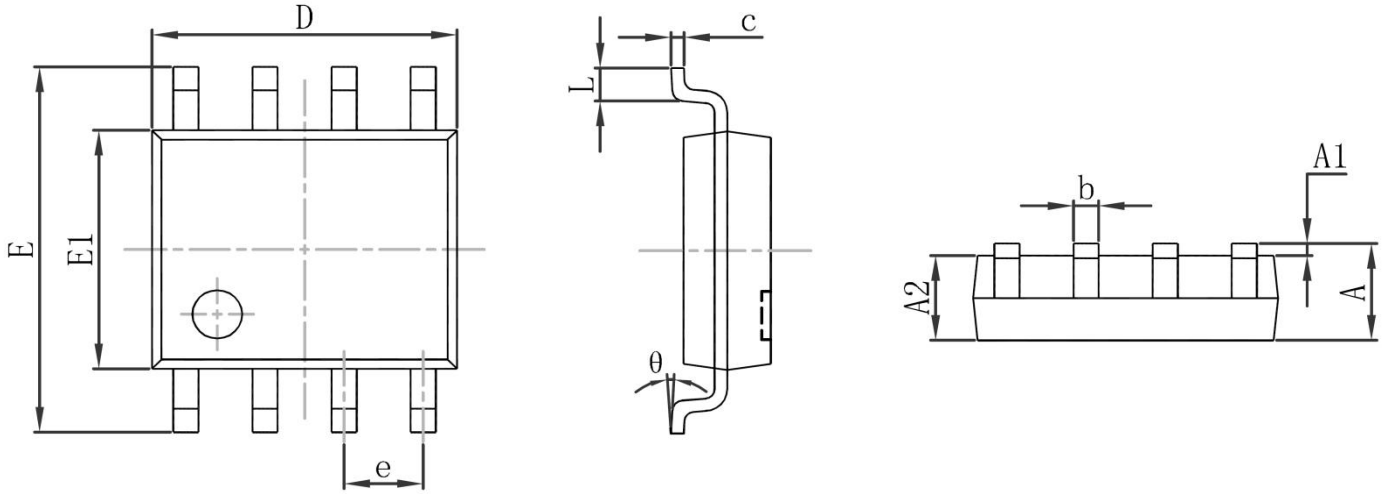
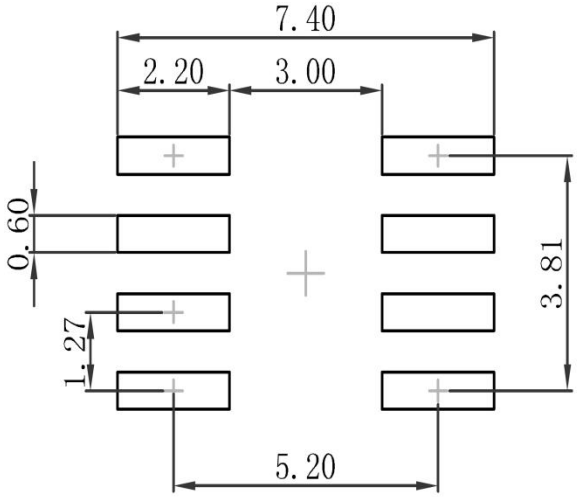
SOP-8 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270(BSC)		0.050（BSC）	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

SOP-8 Suggested Pad Layout



Note:

1.Controlling dimension: in millimeters

2.General tolerance: ±0.05mm

3.The pad layout is for reference purposes only

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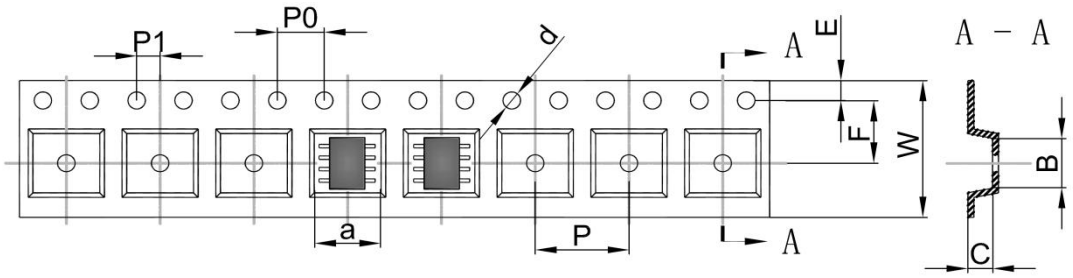
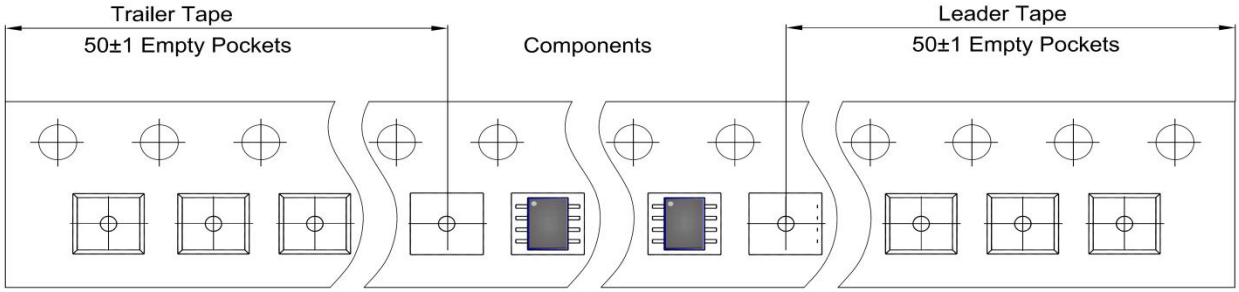
SOP-8 Tape and Reel

SOP-8 Embossed Carrier Tape

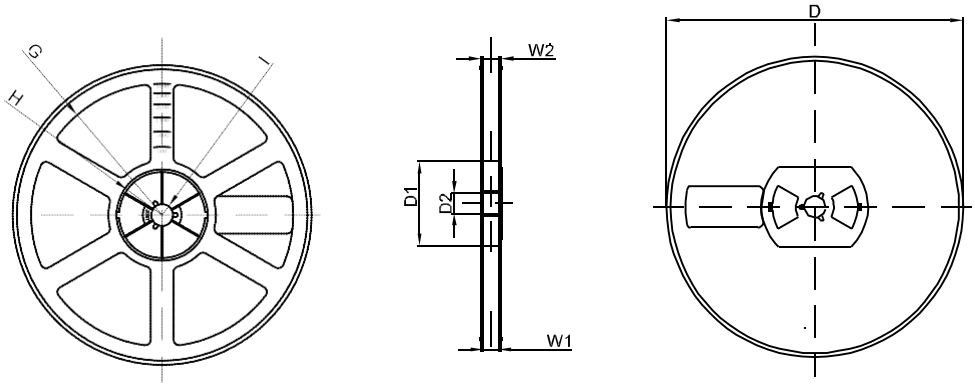


	DIMENSIONS ARE IN MILLIMETER									
TYPE	A	B	C	d	E	F	P0	P	P1	W
SOP-8	6.40	5.40	2.10	Ø1.50	1.75	5.50	4.00	8.00	2.00	12.00
TOLERANCE	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1

SOP-8 Tape Leader and Trailer



SOP-8 Reel



	DIMENSIONS ARE IN MILLIMETER							
REEL OPTION	D	D1	D2	G	H	I	W1	W2
13” DIA	Ø330.00	100.00	13.00	R151.00	R56.00	R6.50	12.40	17.60
TOLERANCE	±2	±1	±1	±1	±1	±1	±1	±1