

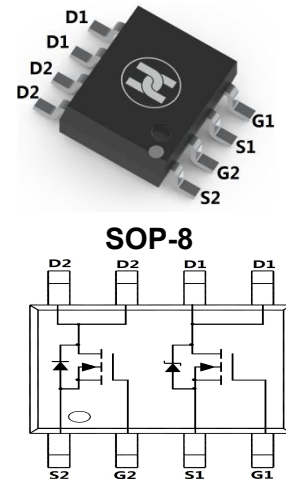
Dual Asymmetric N-Channel MOSFET

FEATURES

- Very Low $R_{DS(on)}$ at 4.5V $V_{GS}:V_{DS}=30V, I_D=11A, R_{DS(ON)} \leq 10.5m\Omega @ V_{GS}=10V$
 $V_{DS}=30V, I_D=11A, R_{DS(ON)} \leq 11.5m\Omega @ V_{GS}=10V$
- Latest Trench Power AlphaMOS (α MOS LV) technology
- Integrated Schottky Diode (SRFET) on Low-Side
- Low Gate Charge and High Current Capability

MECHANICAL DATA

- Case: SOP-8
- Case Material: Molded Plastic. UL flammability
- Classification Rating: 94V-0
- Weight: 0.3 grams (approximate)



MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Max Q1	Max Q2	Unit
Drain-source voltage	V_{DS}	30	30	V
Gate-source voltage	V_{GS}	± 20	± 20	V
Continuous drain current	I_D	$T_A = 25^\circ\text{C}$	11	A
		$T_A = 70^\circ\text{C}$	9	A
Pulsed drain current	I_{DM}	75	74	A
Avalanche current	I_{AS}, I_{AR}	18	15	A
Avalanche energy $L=0.1\text{mH}$	E_{AS}, E_{AR}	16	11	mJ
Power dissipation	P_D	$T_A = 25^\circ\text{C}$	2	W
		$T_A = 70^\circ\text{C}$	1.3	W
Thermal resistance from Junction to ambient	$R_{\theta JA}$	90		$^\circ\text{C/W}$
Thermal resistance from Junction to Lead	$R_{\theta JL}$	40		$^\circ\text{C/W}$
Junction temperature	T_J	150		$^\circ\text{C}$
Storage temperature	T_{STG}	-55 ~ +150		$^\circ\text{C}$

Q1 ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Drain-Source breakdown voltage	$V_{(BR)DSS}^*$	30			V	$V_{GS}=0V, I_D=250\mu\text{A}$
Zero gate voltage drain current	I_{DSS}^*			0.5	mA	$V_{DS}=30V, V_{GS}=0V$
Gate-body leakage current	I_{GSS}^*			± 100	nA	$V_{DS}=0V, V_{GS}=\pm 20V$
Gate-threshold voltage	$V_{GS(th)}^*$	1.4	1.8	2.5	V	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$
On-State Drain Current	$I_{D(ON)}$	30			A	$V_{DS}=5V, V_{GS}=10V$
Drain-source on-resistance	$R_{DS(ON)}^*$		8.3	10.5	m Ω	$V_{GS}=10V, I_D=11A$
			11.8	15	m Ω	$V_{GS}=10V, I_D=11A, T_J=125^\circ\text{C}$
			12.2	15.5	m Ω	$V_{GS}=4.5V, I_D=9A$
Forward transconductance	g_{FS}		52		S	$V_{DS}=5V, I_D=6A$
Diode forward voltage	V_{SD}		0.45	0.65	V	$I_S=0.2A, V_{GS}=0V$
Diode forward current	I_S			2.5	A	
Input capacitance	C_{iss}		605		pF	$V_{DS}=15V, V_{GS}=0V, f=1\text{MHz}$
Output capacitance	C_{oss}		275		pF	
Reverse transfer capacitance	C_{rss}		37		pF	
Gate resistance	R_g	1	2	3	Ω	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$
Total gate charge	Q_g		4.9	8	nC	$V_{GS}=4.5V, V_{DS}=15V, I_D=11A$
Total gate charge			10.2	15	nC	$V_{GS}=10V, V_{DS}=15V, I_D=11A$
Gate-source charge	Q_{gs}		2		nC	
Gate-drain charge	Q_{gd}		2.3		nC	
Turn-on delay time	$t_{d(on)}$		5		nS	$V_{GS}=10V, V_{DS}=15V, R_{GEN}=3\Omega, R_L=1.36\Omega$
Turn-on rise time	t_r		3		nS	
Turn-off delay time	$t_{d(off)}$		17.5		nS	
Turn-off fall time	t_f		3		nS	
Body Diode Reverse Recovery Time	t_{rr}		11		nS	
Body Diode Reverse Recovery Charge	Q_{rr}		12.5		nC	$I_F=11A, di/dt=100A/\mu\text{s}$

*Pulse test ; Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 0.5\%$.

Dual Asymmetric N-Channel MOSFET

Q1-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

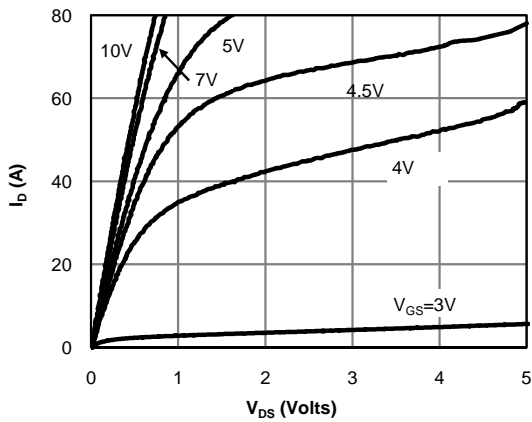


Fig 1: On-Region Characteristics

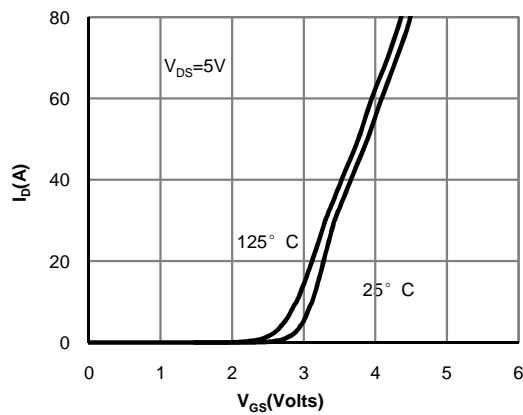


Figure 2: Transfer Characteristics

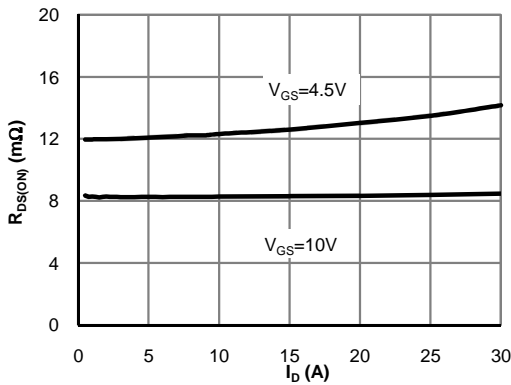


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

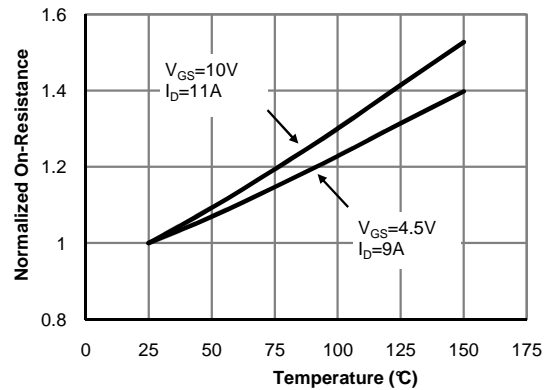


Figure 4: On-Resistance vs. Junction Temperature

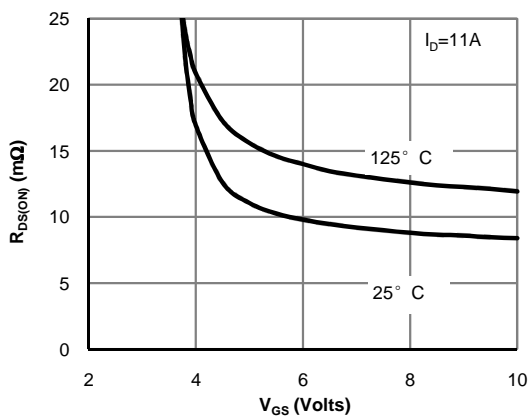


Figure 5: On-Resistance vs. Gate-Source Voltage

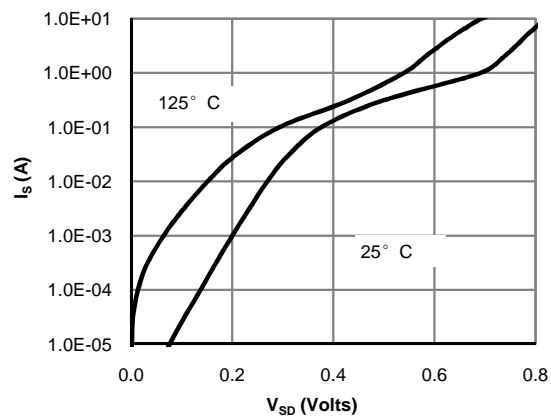


Figure 6: Body-Diode Characteristics

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Q1-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

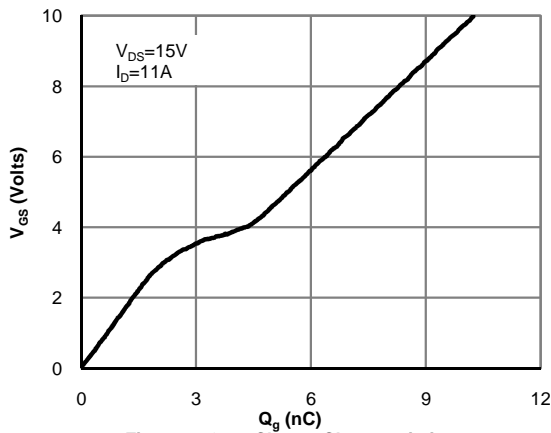


Figure 7: Gate-Charge Characteristics

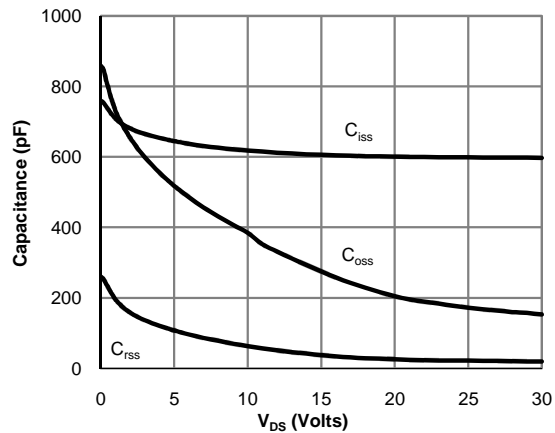
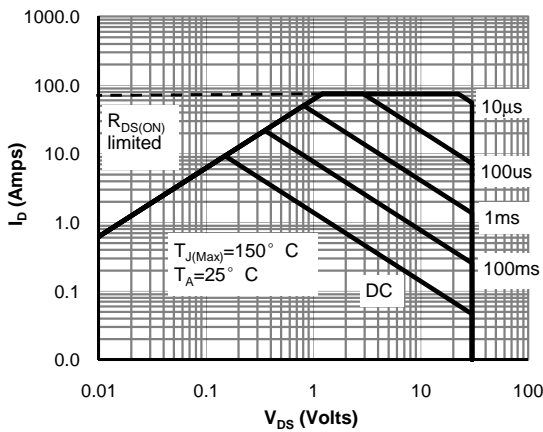


Figure 8: Capacitance Characteristics



VGS > or equal to 4.5V
Figure 9: Maximum Forward Biased Safe Operating Area

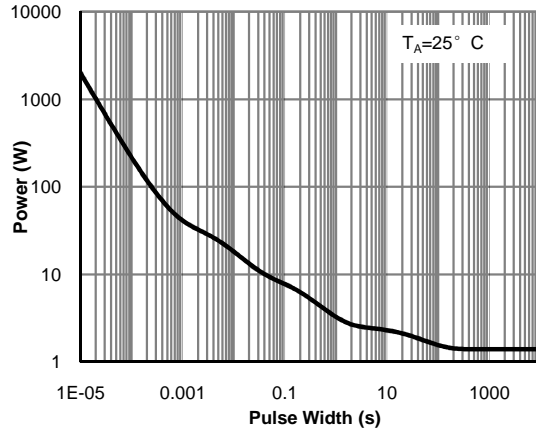


Figure 10: Single Pulse Power Rating Junction-to-Ambient

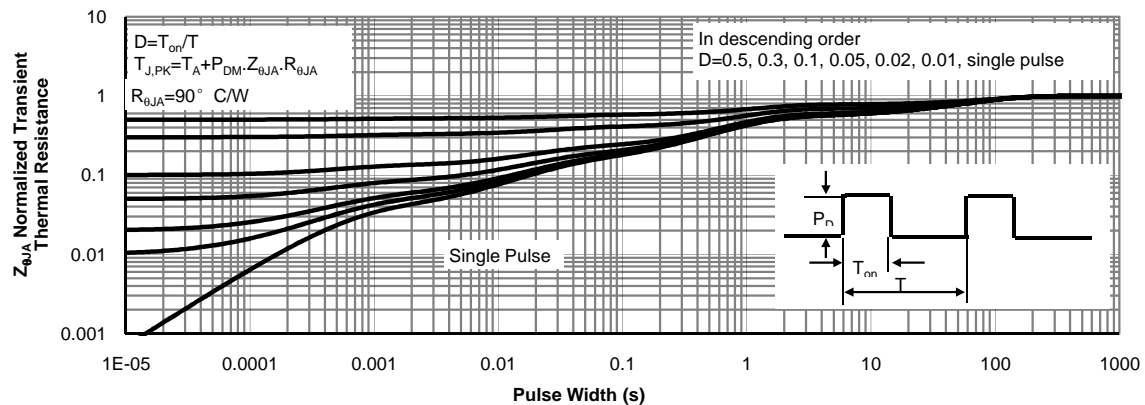


Figure 11: Normalized Maximum Transient Thermal Impedance

Dual Asymmetric N-Channel MOSFET
Q2 ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Drain-Source breakdown voltage	V _{(BR)DSS} *	30			V	V _{GS} =0V, I _D =250μA
Zero gate voltage drain current	I _{DSS} *			1	μA	V _{DS} =30V, V _{GS} =0V
Gate-body leakage current	I _{GSS} *			±100	nA	V _{DS} =0V, V _{GS} =±20V
Gate-threshold voltage	V _{GS(th)} *	1.4	1.8	2.2	V	V _{DS} =V _{GS} , I _D =250μA
Drain-source on-resistance	R _{DS(ON)} *		9	11.5	mΩ	V _{GS} =10V, I _D =11A
			12.4	15.8	mΩ	V _{GS} =10V, I _D =11A, T _J =125°C
			12.8	16.5	mΩ	V _{GS} =4.5V, I _D =9A
Forward transconductance	g _{FS}		40		S	V _{DS} =5V, I _D =11A
Diode forward voltage	V _{SD}		0.72	1	V	I _S =1A, V _{GS} =0V
Diode forward current	I _S			2.5	A	
Input capacitance	C _{iss}		542		pF	V _{DS} =15V, V _{GS} =0V, f=1MHz
Output capacitance	C _{oss}		233		pF	
Reverse transfer capacitance	C _{rss}		31		pF	
Gate resistance	R _g	1	2	3	Ω	V _{DS} =0V, V _{GS} =0V, f=1MHz
Total gate charge	Q _g		4.3	6	nC	V _{GS} =4.5V, V _{DS} =15V, I _D =11A
Total gate charge			9	12.5	nC	
Gate-source charge	Q _{gs}		2.2		nC	V _{GS} =10V, V _{DS} =15V, I _D =11A
Gate-drain charge	Q _{gd}		1.7		nC	
Turn-on delay time	t _{d(on)}		4		nS	
Turn-on rise time	t _r		3.5		nS	V _{GS} =10V, V _{DS} =15V, R _{GEN} =3Ω, R _L =1.36Ω
Turn-off delay time	t _{d(off)}		18		nS	
Turn-off fall time	t _f		3		nS	
Body Diode Reverse Recovery Time	t _{rr}		9.7		nS	I _F =11A, dI/dt=500A/μs
Body Diode Reverse Recovery Charge	Q _{rr}		11.5		nC	I _F =11A, dI/dt=500A/μs

*Pulse test ; Pulse width ≤300μs, Duty cycle ≤ 0.5% .

Dual Asymmetric N-Channel MOSFET

Q2-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

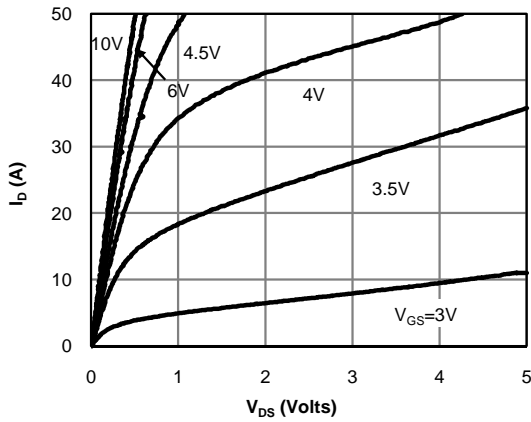


Fig 1: On-Region Characteristics

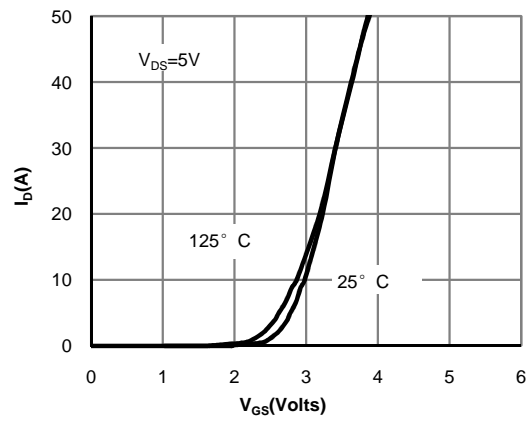


Figure 2: Transfer Characteristics

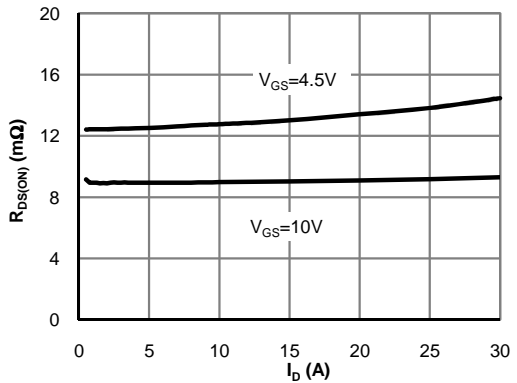


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

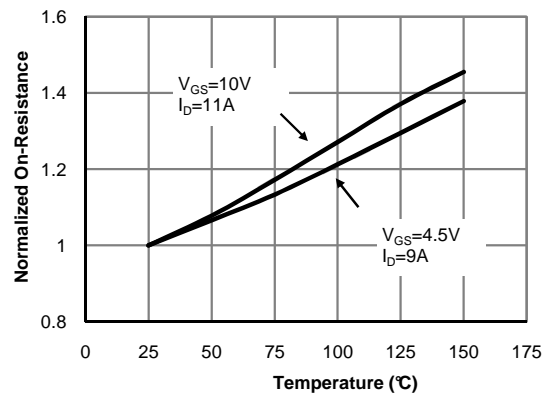


Figure 4: On-Resistance vs. Junction Temperature

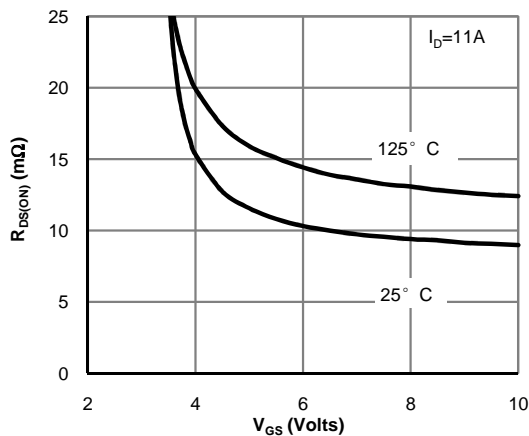


Figure 5: On-Resistance vs. Gate-Source Voltage

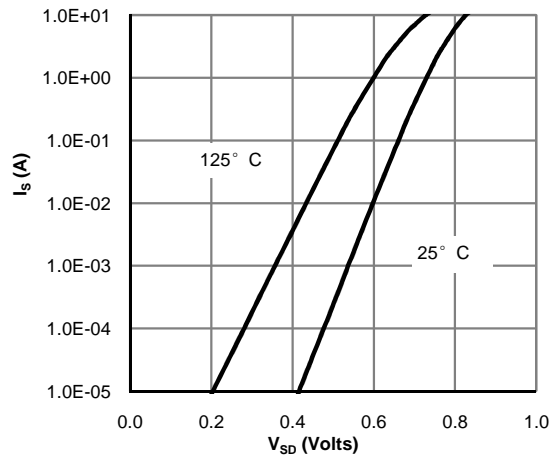


Figure 6: Body-Diode Characteristics

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Q2-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

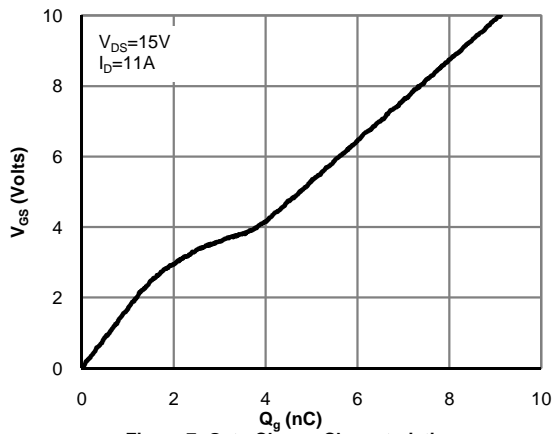


Figure 7: Gate-Charge Characteristics

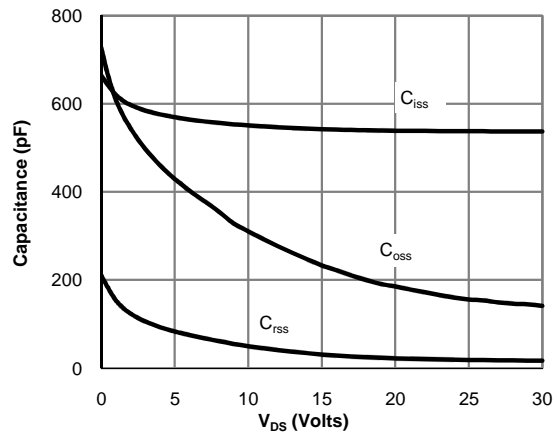


Figure 8: Capacitance Characteristics

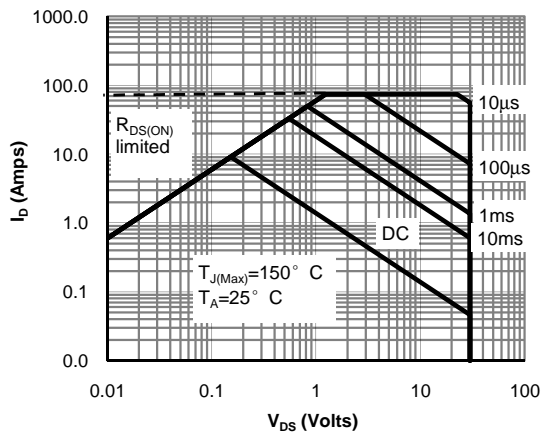


Figure 9: Maximum Forward Biased Safe Operating Area

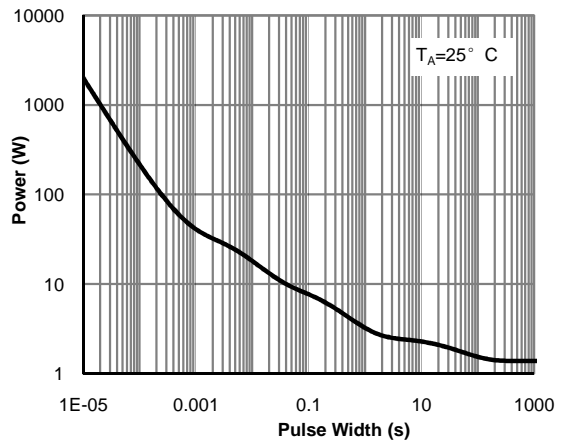


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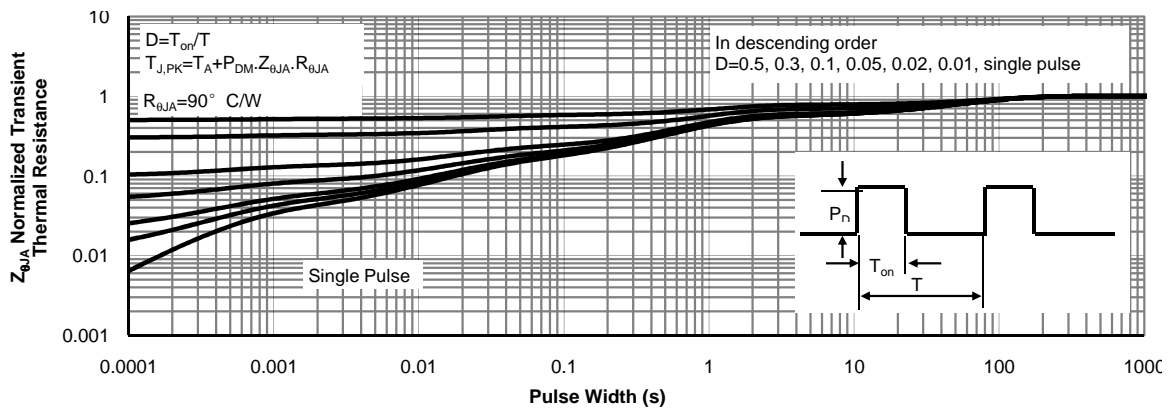
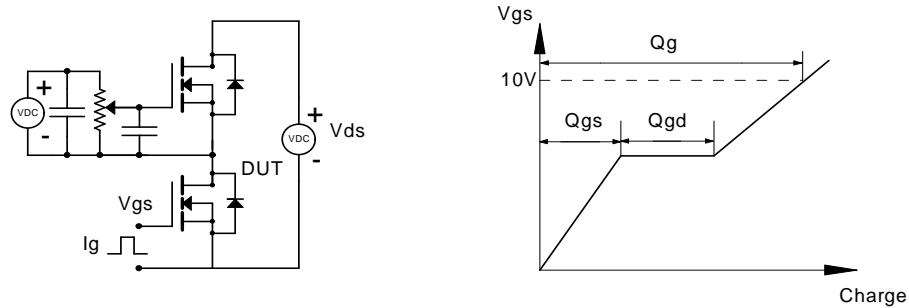


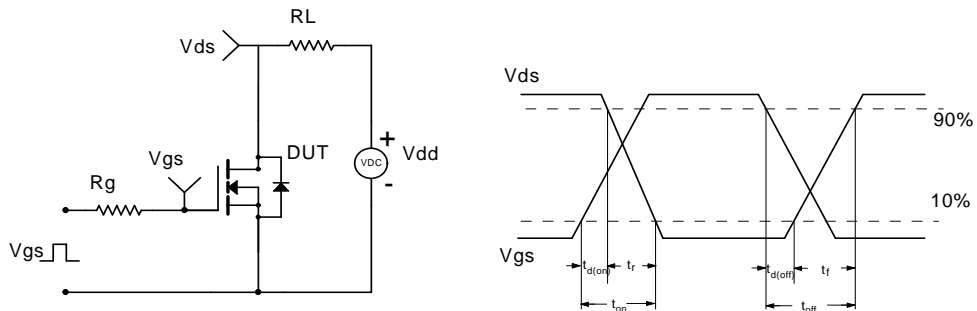
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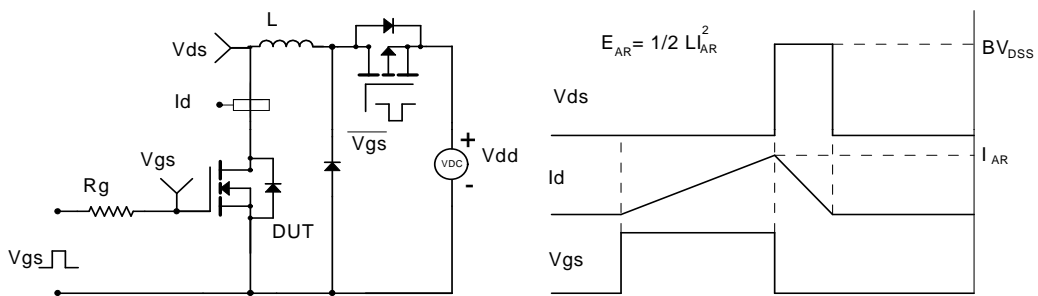
Gate Charge Test Circuit & Waveform



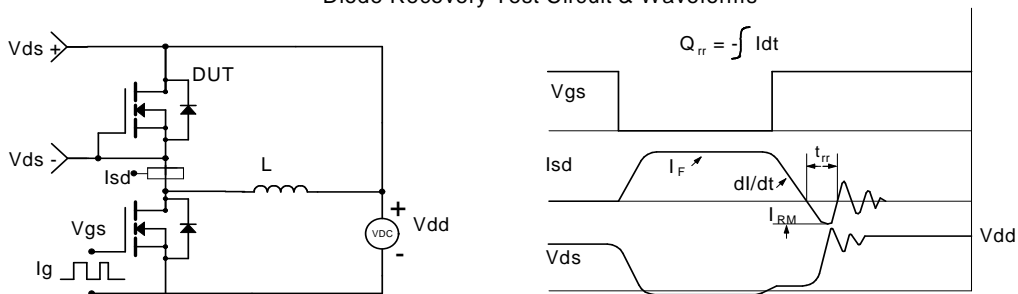
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

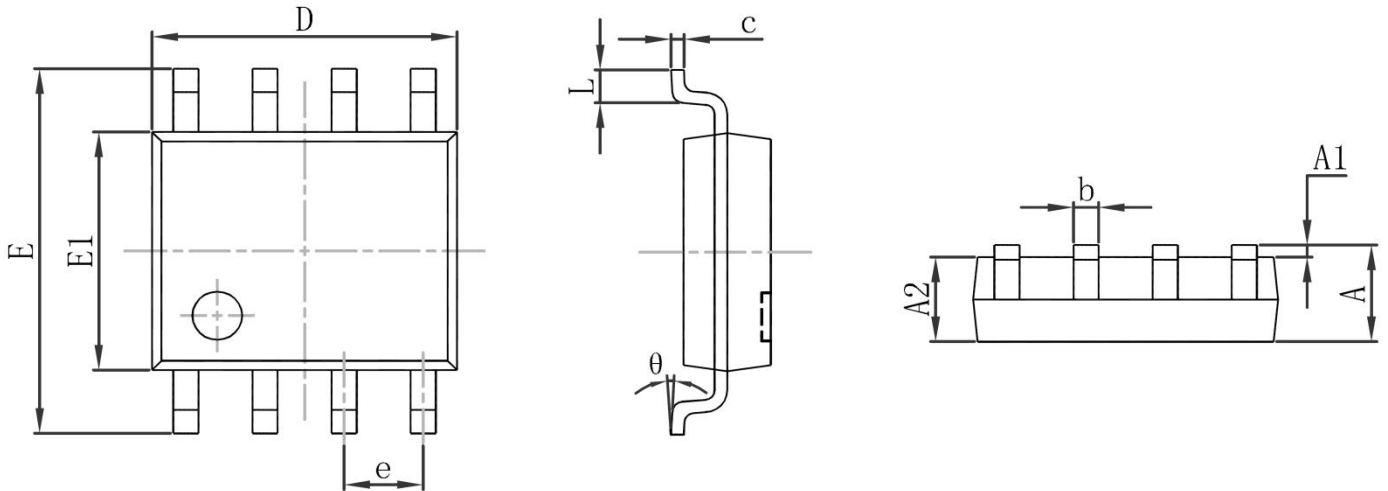


Diode Recovery Test Circuit & Waveforms



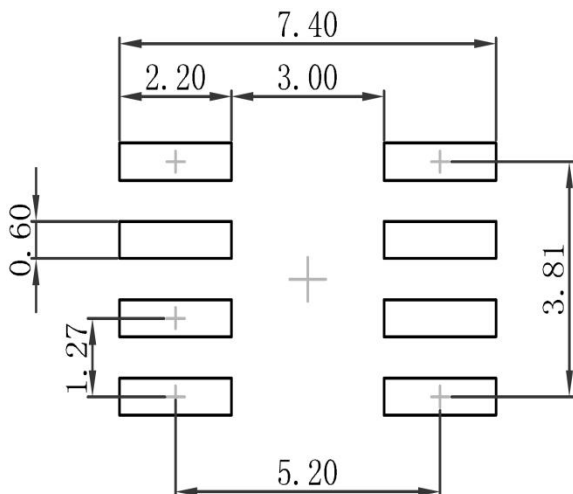
Dual Asymmetric N-Channel MOSFET

SOP-8 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270(BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

SOP-8 Suggested Pad Layout



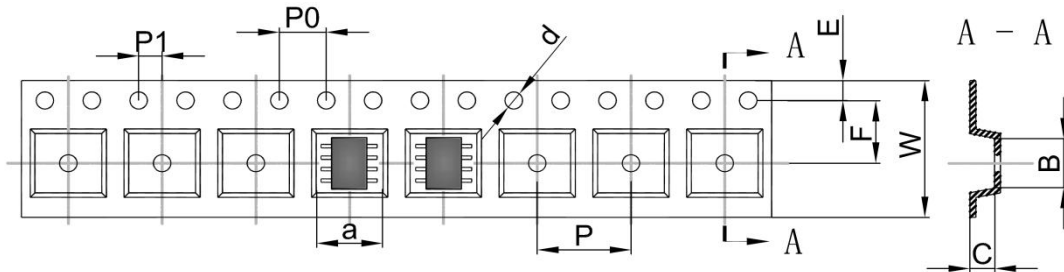
Note:

1. Controlling dimension: in millimeters
2. General tolerance: $\pm 0.05\text{mm}$
3. The pad layout is for reference purposes only

Dual Asymmetric N-Channel MOSFET

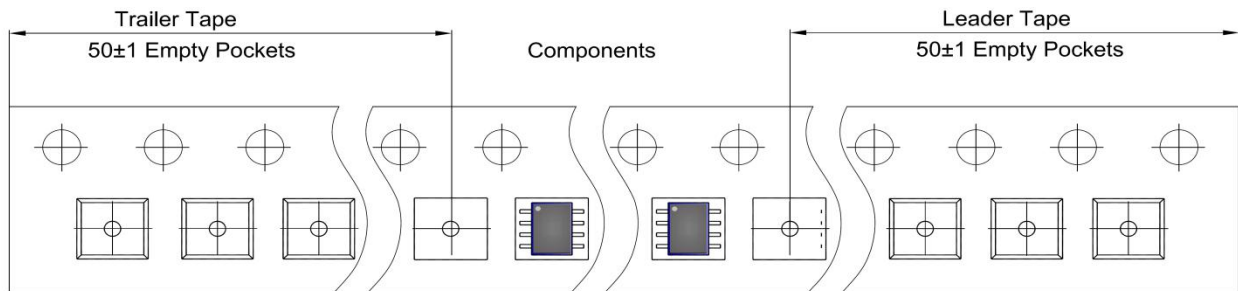
SOP-8 Tape and Reel

SOP-8 Embossed Carrier Tape

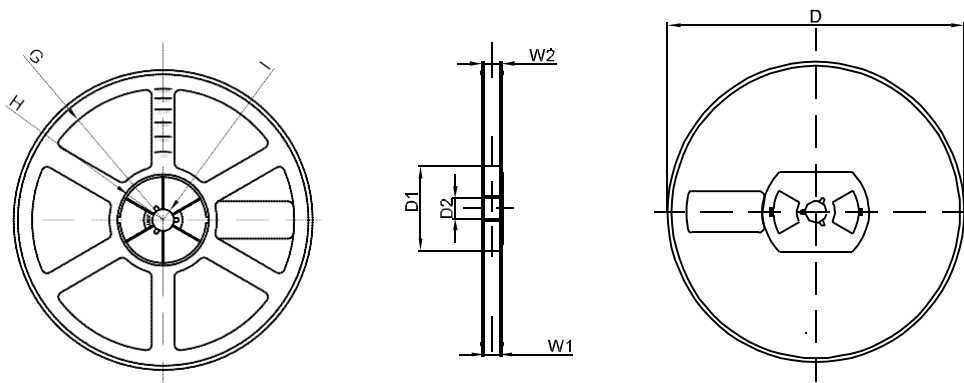


DIMENSIONS ARE IN MILLIMETER										
TYPE	A	B	C	d	E	F	P0	P	P1	W
SOP-8	6.40	5.40	2.10	Ø1.50	1.75	5.50	4.00	8.00	2.00	12.00
TOLERANCE	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1

SOP-8 Tape Leader and Trailer



SOP-8 Reel



DIMENSIONS ARE IN MILLIMETER								
REEL OPTION	D	D1	D2	G	H	I	W1	W2
13" DIA	Ø330.00	100.00	13.00	R151.00	R56.00	R6.50	12.40	17.60
TOLERANCE	±2	±1	±1	±1	±1	±1	±1	±1