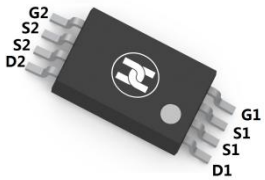
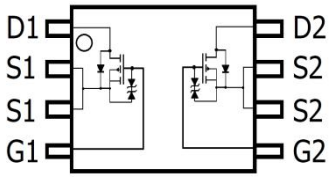
DUAL P-CHANNEL ENHANCEMENT MODE FET



FEATURES

- Ultra low on-resistance:V_{DS}=-20V,I_D=-4.5A,$R_{DS(ON)}$≤42mΩ@V_{GS}=-4.5V
- Low gate charge
- ESD protected
- For load switch or in PWM applications
- Surface Mount device

TSSOP-8



MECHANICAL DATA

- Case: TSSOP-8
- Case Material: Molded Plastic. UL flammability
- Classification Rating: 94V-0
- Weight: not available

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-source voltage		V_{DS}	-20	V
Gate-source voltage		V_{GS}	±8	V
Continuous drain current	T_A = 25°C	I_D	-4.5	A
	T_A = 70°C		-3.6	A
Pulsed drain current		I_{DM}	-30	A
Power dissipation	T_A = 25°C	P_D	1.5	W
	T_A = 70°C		0.96	W
Thermal resistance from Junction to ambient		$R_{\theta JA}$	130	°C/W
Thermal resistance from Junction to Lead		$R_{\theta JL}$	83	°C/W
Junction temperature		T_J	150	°C
Storage temperature		T_{STG}	-55 ~+150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Drain-Source breakdown voltage	$V_{(BR)DSS}$*	-20			V	V_{GS}=0V, I_D=250μA
Zero gate voltage drain current	I_{DSS}*			-1	μA	V_{DS}=-20V, V_{GS}=0V
Gate-body leakage current	I_{GSS}*			±10	μA	V_{DS}=0V, V_{GS}=±8V
Gate-threshold voltage	$V_{GS(th)}$*	-0.3	-0.57	-0.9	V	V_{DS}=V_{GS}, I_D=-250μA
On-State Drain Current	$I_{D(ON)}$*	-30			A	V_{DS}=-5V, V_{GS}=-4.5V
Drain-source on-resistance	$R_{DS(ON)}$*		35	42	mΩ	V_{GS}=-4.5V, I_D=-4.5A
			49	59	mΩ	V_{GS}=-4.5V,I_D=-4.5A,T_J=125°C
			43	54	mΩ	V_{GS}=-2.5V, I_D=-4A
			54	68	mΩ	V_{GS}=-1.8V, I_D=-3A
Forward transconductance	g_{FS}		20		S	V_{DS}=-5V, I_D=-4.5A
Diode forward voltage	V_{SD}		-0.64	-1	V	I_S=-1A, V_{GS}=0V
Diode forward current	I_S			-2	A	
Input capacitance	C_{iss}	600	751	905	pF	V_{DS}=-10V, V_{GS}=0V, f=1MHz
Output capacitance	C_{oss}	80	115	150	pF	
Reverse transfer capacitance	C_{rss}	48	80	115	pF	
Gate resistance	R_g	6	13	20	Ω	V_{DS}=0V, V_{GS}=0V, f=1MHz
Total gate charge	Q_g	7.4	9.3	11	nC	V_{GS}=-4.5V,V_{DS}=-10V,I_D=-4.5A
Gate-source charge	Q_{gs}	0.8	1	1.2	nC	
Gate-drain charge	Q_{gd}	1.3	2.2	3.1	nC	
Turn-on delay time	$t_{d(on)}$		13		nS	V_{GS}=-4.5V, V_{DS}=-10V, R_{GEN}=3Ω,R_L=2.2Ω
Turn-on rise time	t_r		9		nS	
Turn-off delay time	$t_{d(off)}$		19		nS	
Turn-off fall time	t_f		29		nS	
Body Diode Reverse Recovery Time	t_{rr}	20	26	32	nS	I_F=-4.5A, dI/dt=500A/μs
Body Diode Reverse Recovery Charge	Q_{rr}	40	51	62	nC	I_F=-4.5A, dI/dt=500A/μs

*Pulse test ; Pulse width ≤300μs, Duty cycle ≤ 0.5% .

DUAL P-CHANNEL ENHANCEMENT MODE FET

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

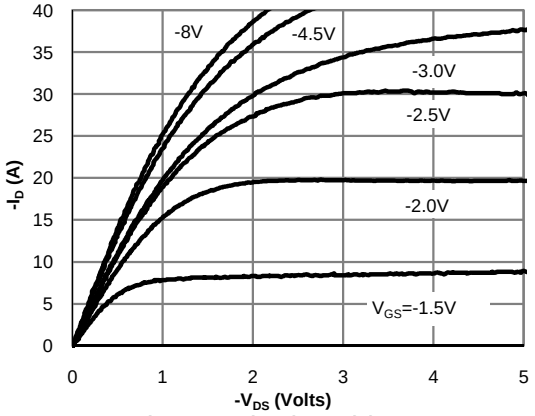


Fig 1: On-Region Characteristics

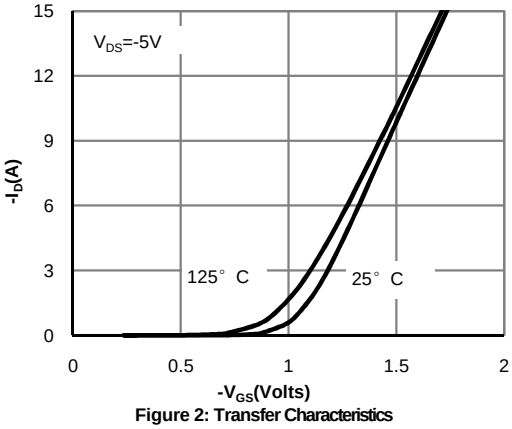


Figure 2: Transfer Characteristics

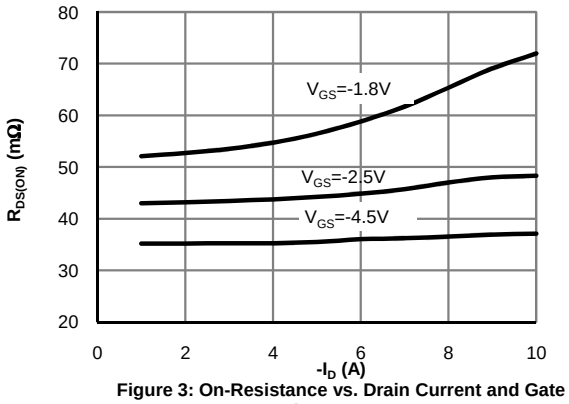


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

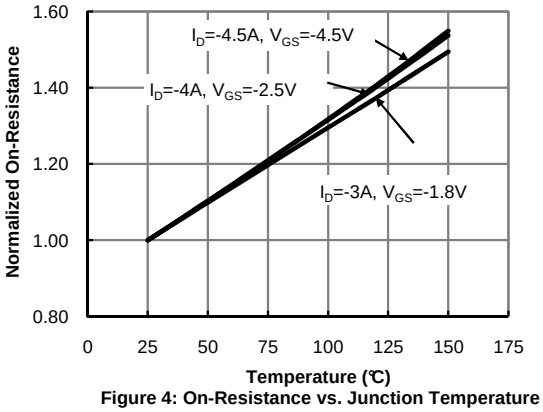


Figure 4: On-Resistance vs. Junction Temperature

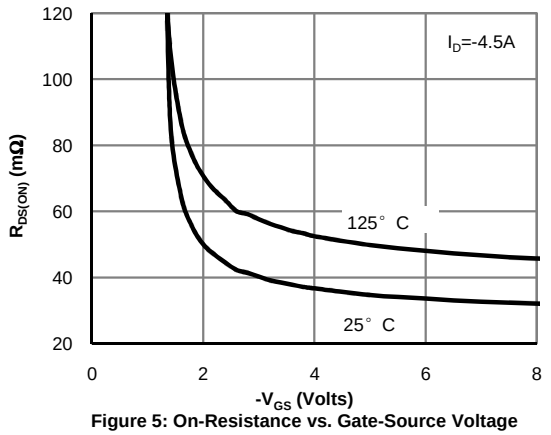


Figure 5: On-Resistance vs. Gate-Source Voltage

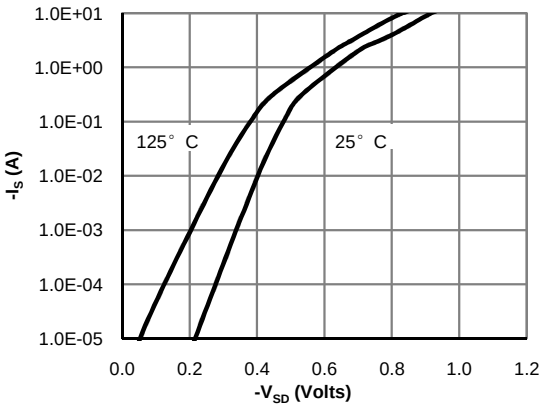


Figure 6: Body-Diode Characteristics

DUAL P-CHANNEL ENHANCEMENT MODE FET

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

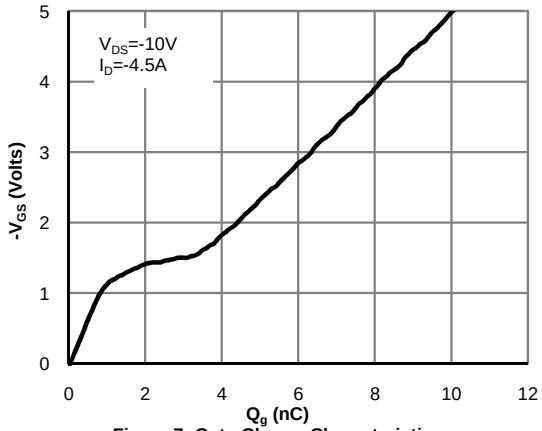


Figure 7: Gate-Charge Characteristics

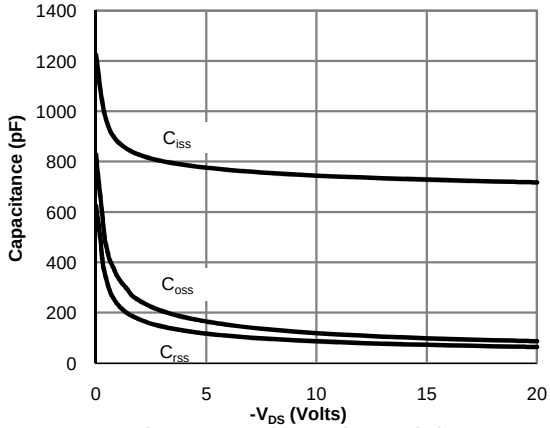


Figure 8: Capacitance Characteristics

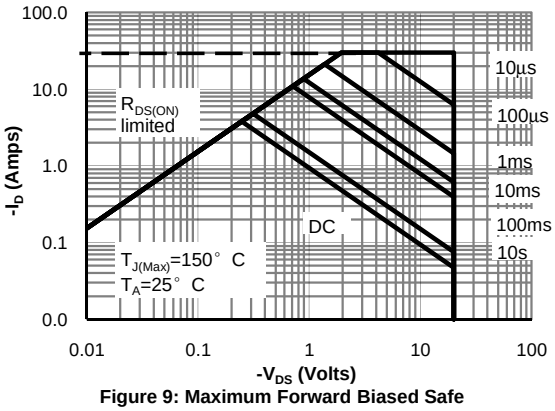


Figure 9: Maximum Forward Biased Safe Operating Area

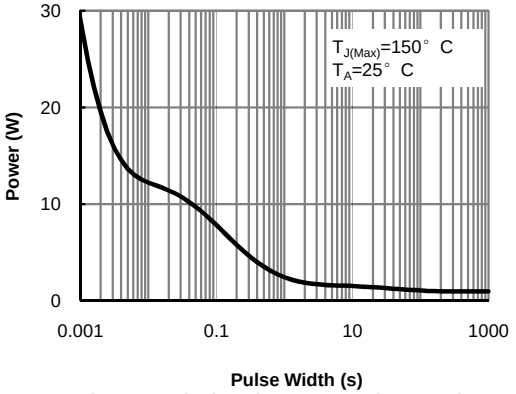


Figure 10: Single Pulse Power Rating Junction-to-Ambient

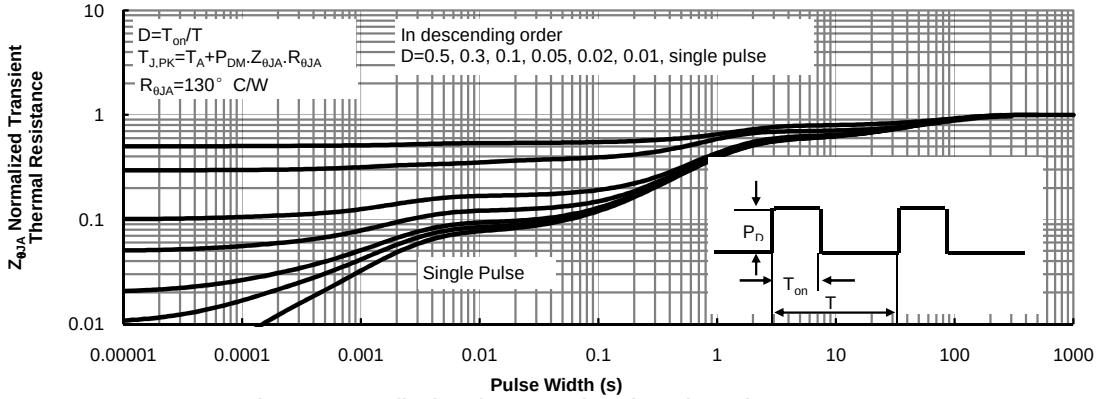
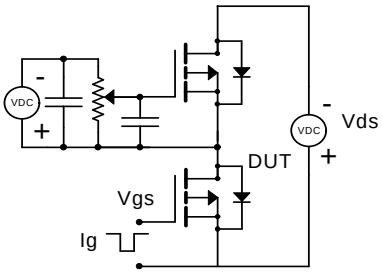
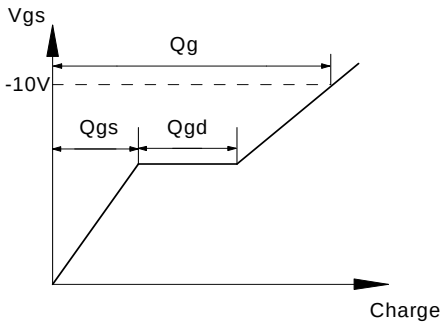


Figure 11: Normalized Maximum Transient Thermal Impedance

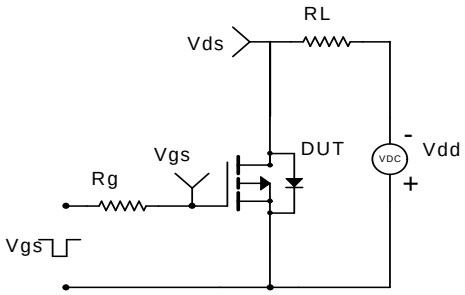
DUAL P-CHANNEL ENHANCEMENT MODE FET

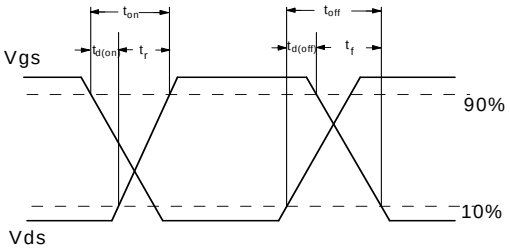
Gate Charge Test Circuit & Waveform



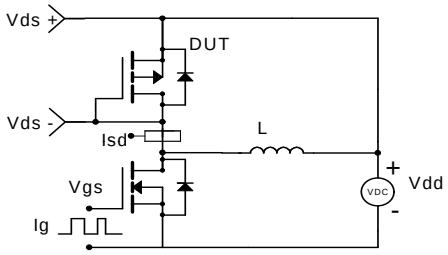


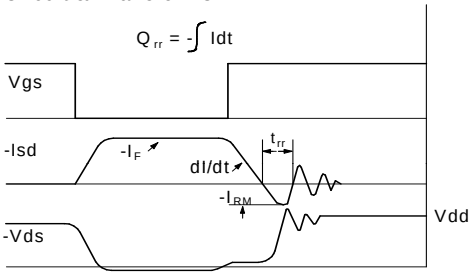
Resistive Switching Test Circuit & Waveforms





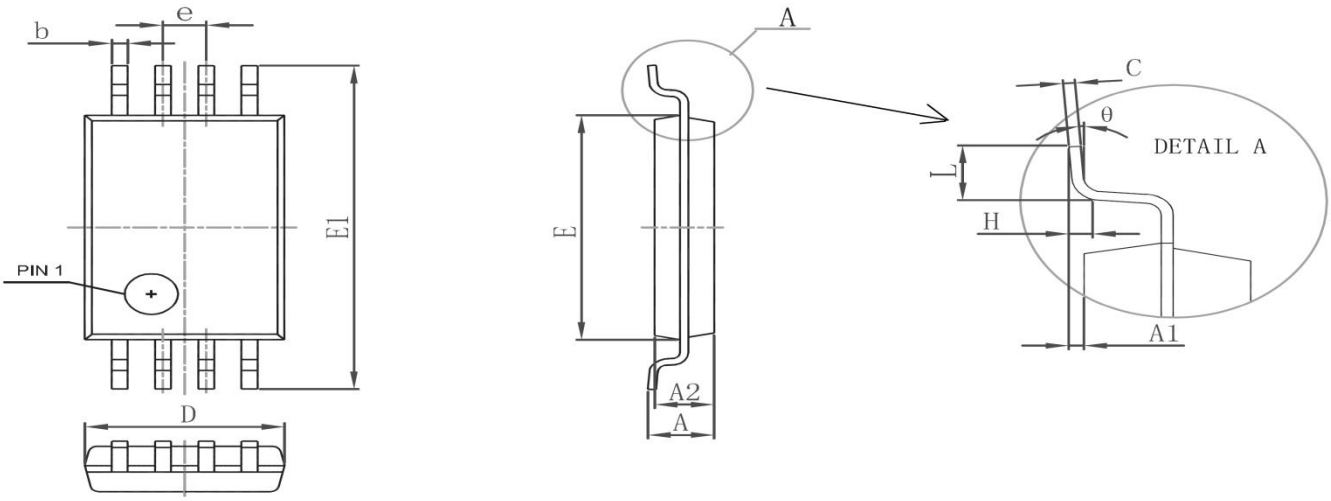
Diode Recovery Test Circuit & Waveforms





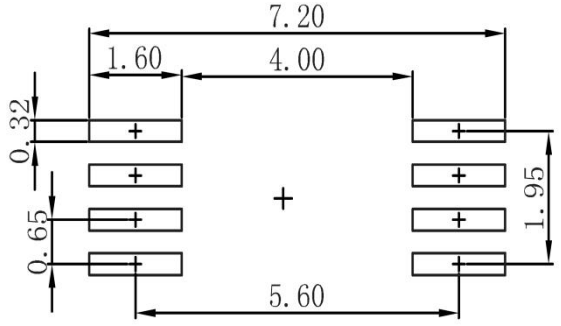
DUAL P-CHANNEL ENHANCEMENT MODE FET

TSSOP-8 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
D	2.900	3.100	0.114	0.122
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65(BSC)		0.026(BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

TSSOP-8 Suggested Pad Layout



Note:

1.Controlling dimension: in millimeters

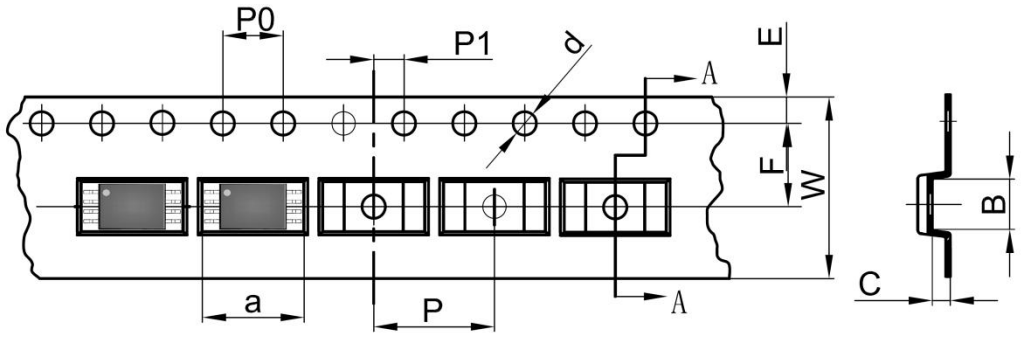
2.General tolerance: ±0.05mm

3.The pad layout is for reference purposes only

DUAL P-CHANNEL ENHANCEMENT MODE FET

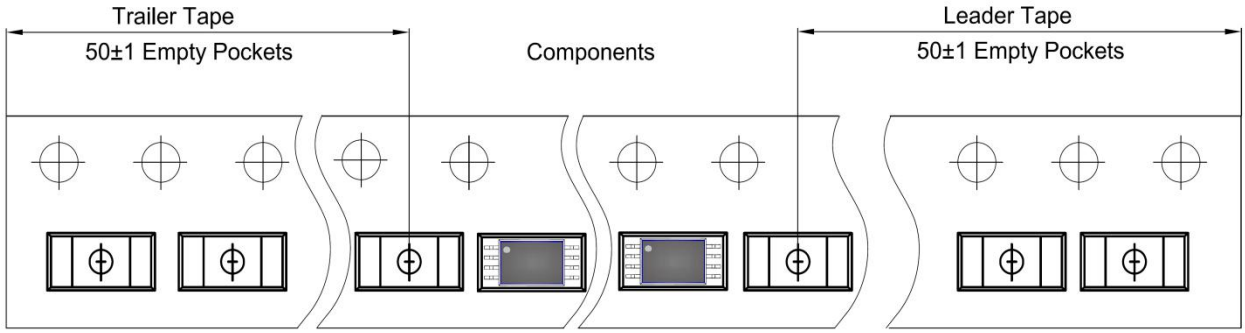
TSSOP-8 Tape and Reel

TSSOP-8 Embossed Carrier Tape

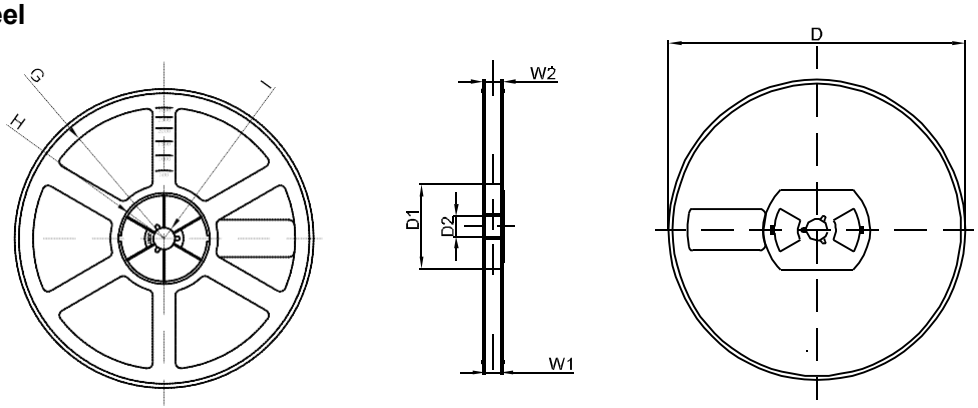


	DIMENSIONS ARE IN MILLIMETER									
TYPE	a	B	C	d	E	F	P0	P	P1	W
TSSOP-8	6.76	3.30	1.20	Ø1.50	1.75	5.50	4.00	8.00	2.00	12.00
TOLERANCE	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1

TSSOP-8 Tape Leader and Trailer



TSSOP-8 Reel



	DIMENSIONS ARE IN MILLIMETER							
REEL OPTION	D	D1	D2	G	H	I	W1	W2
13” DIA	Ø330.00	100.00	13.00	R151.00	R56.00	R6.50	12.40	17.60
TOLERANCE	±2	±1	±1	±1	±1	±1	±1	±1