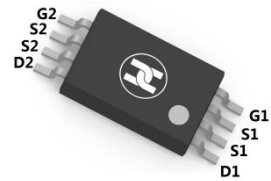
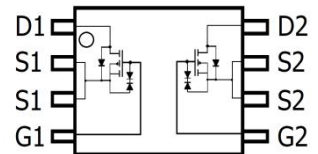


DUAL P-CHANNEL ENHANCEMENT MODE FET

FEATURES

- Ultra low on-resistance: $V_{DS}=-12V, I_D=-7A, R_{DS(ON)} \leq 18m\Omega @ V_{GS}=-4.5V$
- Low gate charge
- ESD protected
- Surface Mount device


TSSOP-8


MECHANICAL DATA

- Case: TSSOP-8
- Case Material: Molded Plastic. UL flammability
- Classification Rating: 94V-0
- Weight: not available

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	-12	V
Gate-source voltage	V_{GS}	± 8	V
Continuous drain current	I_D	$T_A = 25^\circ\text{C}$	A
		$T_A = 70^\circ\text{C}$	A
Pulsed drain current	I_{DM}	-30	A
Power dissipation	P_D	$T_A = 25^\circ\text{C}$	W
		$T_A = 70^\circ\text{C}$	W
Thermal resistance from Junction to ambient	$R_{\theta JA}$	125	$^\circ\text{C/W}$
Thermal resistance from Junction to Lead	$R_{\theta JL}$	75	$^\circ\text{C/W}$
Junction temperature	T_J	150	$^\circ\text{C}$
Storage temperature	T_{STG}	-55 ~ +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Drain-Source breakdown voltage	$V_{(BR)DSS}^*$	-12			V	$V_{GS}=0V, I_D=250\mu A$
Zero gate voltage drain current	I_{DSS}^*			-1	μA	$V_{DS}=-9.6V, V_{GS}=0V$
Gate-body leakage current	I_{GSS}^*			± 1	μA	$V_{DS}=0V, V_{GS}=\pm 4.5V$
				± 10	μA	$V_{DS}=0V, V_{GS}=\pm 8V$
Gate-threshold voltage	$V_{GS(th)}^*$	-0.3	-0.55	-1	V	$V_{DS}=V_{GS}, I_D=-250\mu A$
On-State Drain Current	$I_{D(ON)}^*$	-30			A	$V_{DS}=-5V, V_{GS}=-4.5V$
Drain-source on-resistance	$R_{DS(ON)}^*$		15	18	m Ω	$V_{GS}=-4.5V, I_D=-7A$
			19	23	m Ω	$V_{GS}=-4.5V, I_D=-7A, T_J=125^\circ\text{C}$
			18	22	m Ω	$V_{GS}=-2.5V, I_D=-6A$
			22	29	m Ω	$V_{GS}=-1.8V, I_D=-5A$
			28		m Ω	$V_{GS}=-1.5V, I_D=-1A$
Forward transconductance	g_{FS}		34		S	$V_{DS}=-5V, I_D=-4.7A$
Diode forward voltage	V_{SD}		-0.78	-1	V	$I_S=-1A, V_{GS}=0V$
Diode forward current	I_S			-2.5	A	
Input capacitance	C_{iss}		3960	4750	pF	$V_{DS}=-6V, V_{GS}=0V, f=1\text{MHz}$
Output capacitance	C_{oss}		910		pF	
Reverse transfer capacitance	C_{rss}		757		pF	
Gate resistance	R_g		6.9	8.5	Ω	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$
Total gate charge	Q_g		36.6	44	nC	$V_{GS}=-4.5V, V_{DS}=-6V, I_D=-7A$
Gate-source charge	Q_{gs}		3.4		nC	
Gate-drain charge	Q_{gd}		10		nC	
Turn-on delay time	$t_{d(on)}$		15		nS	$V_{GS}=-4.5V, V_{DS}=-6V, R_{GEN}=3\Omega, R_L=0.86\Omega$
Turn-on rise time	t_r		43		nS	
Turn-off delay time	$t_{d(off)}$		158		nS	
Turn-off fall time	t_f		95		nS	
Body Diode Reverse Recovery Time	t_{rr}		49	60	nS	$I_F=-7A, dI/dt=100A/\mu s$
Body Diode Reverse Recovery Charge	Q_{rr}		19.4		nC	$I_F=-7A, dI/dt=100A/\mu s$

*Pulse test ; Pulse width $\leq 300\mu s$, Duty cycle $\leq 0.5\%$.

DUAL P-CHANNEL ENHANCEMENT MODE FET

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

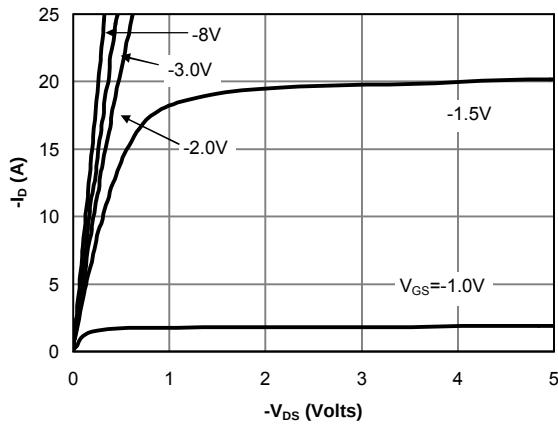


Fig 1: On-Region Characteristics

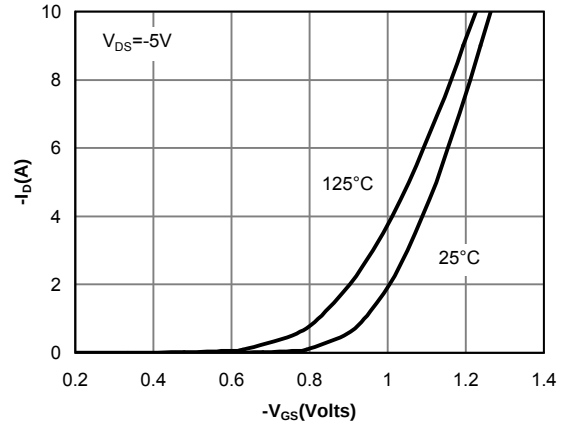


Figure 2: Transfer Characteristics

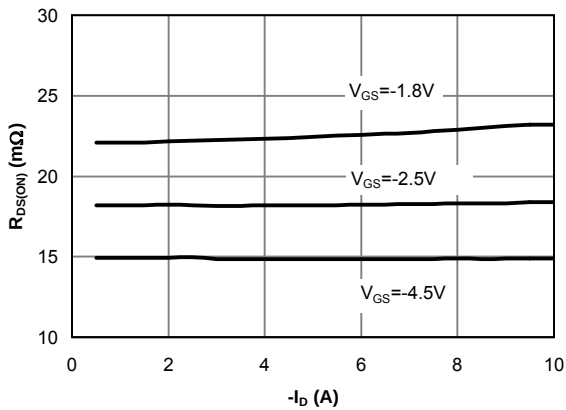


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

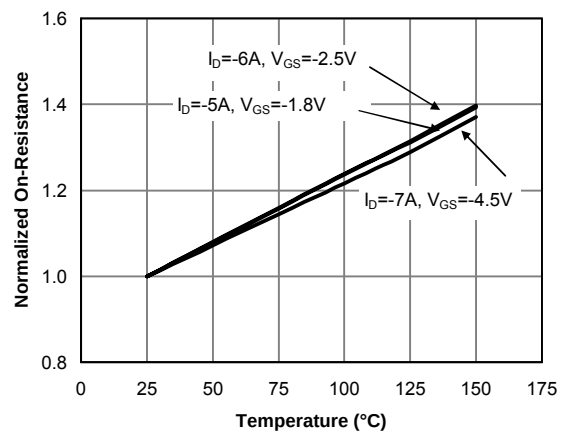


Figure 4: On-Resistance vs. Junction Temperature

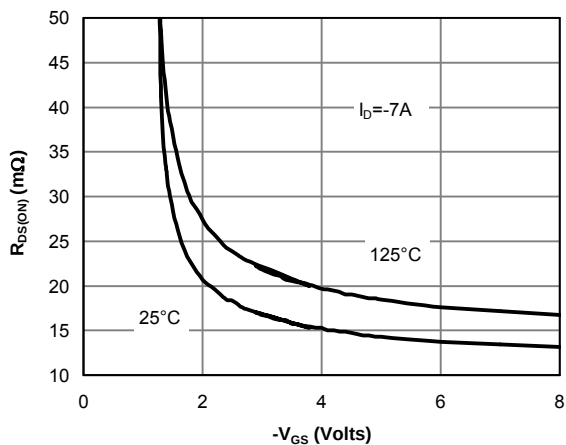


Figure 5: On-Resistance vs. Gate-Source Voltage

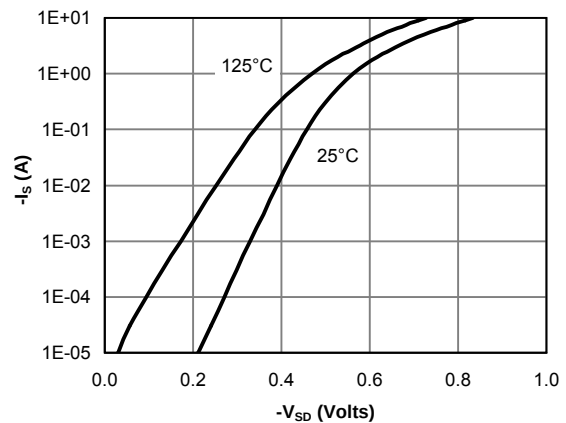


Figure 6: Body-Diode Characteristics

DUAL P-CHANNEL ENHANCEMENT MODE FET

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

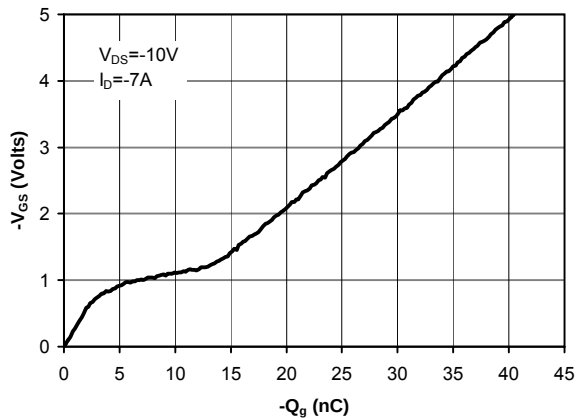


Figure 7: Gate-Charge Characteristics

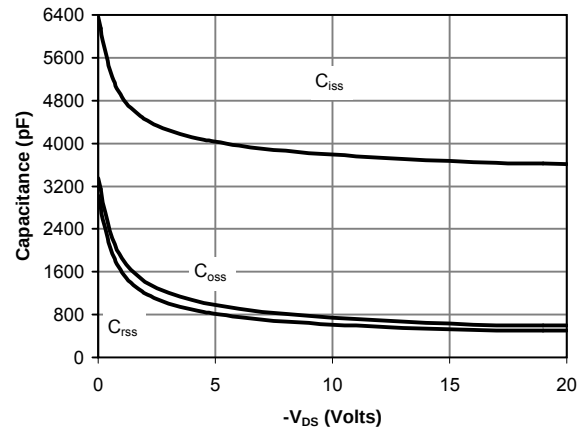


Figure 8: Capacitance Characteristics

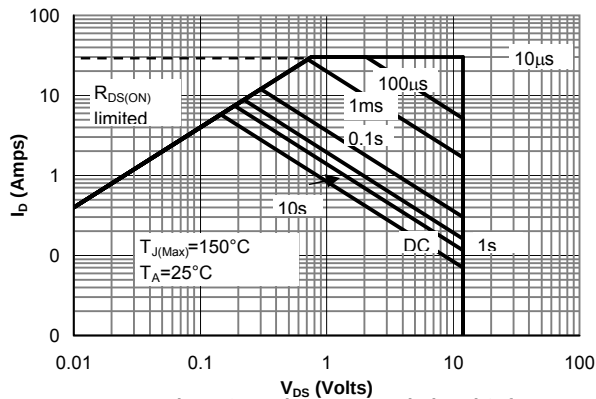


Figure 9: Maximum Forward Biased Safe Operating Area

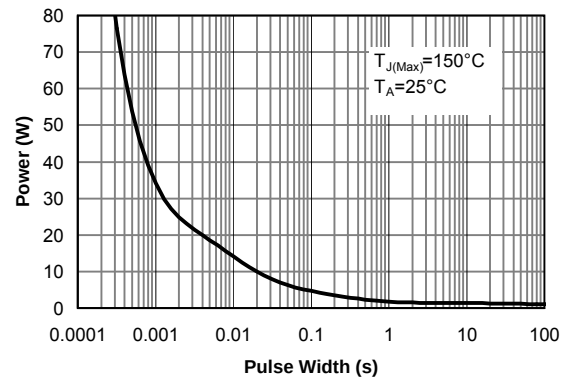


Figure 10: Single Pulse Power Rating Junction-to-Ambient

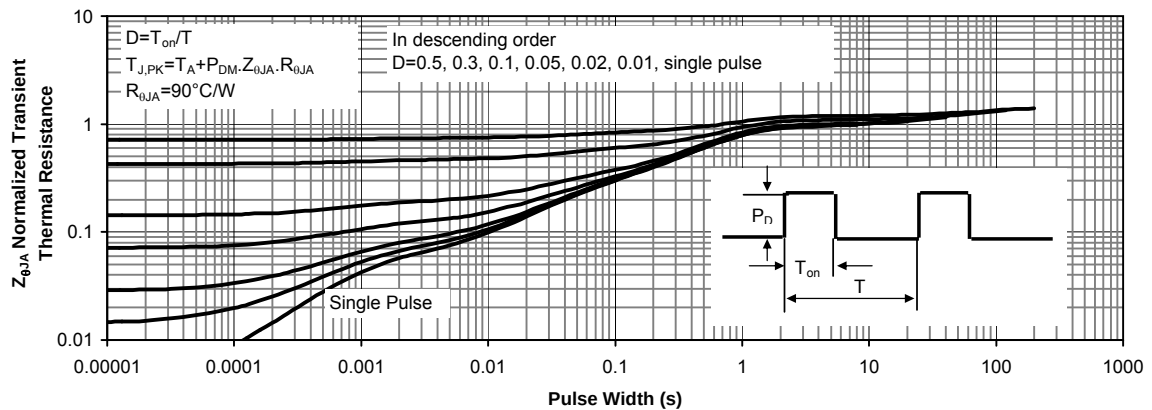
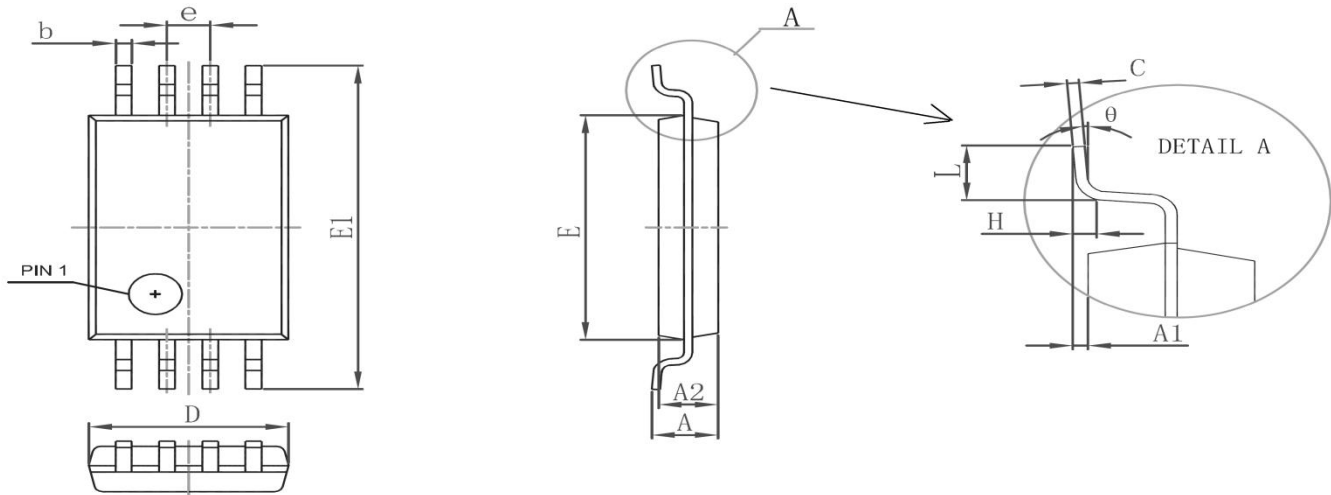


Figure 11: Normalized Maximum Transient Thermal Impedance

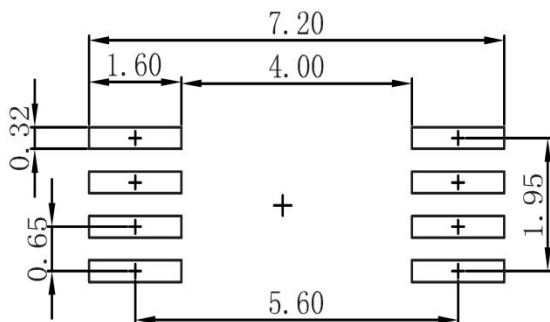
DUAL P-CHANNEL ENHANCEMENT MODE FET

TSSOP-8 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
D	2.900	3.100	0.114	0.122
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65(BSC)		0.026(BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

TSSOP-8 Suggested Pad Layout



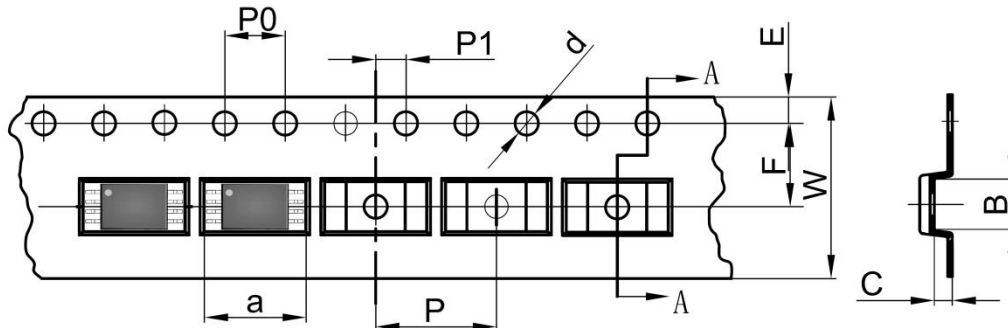
Note:

1. Controlling dimension: in millimeters
2. General tolerance: $\pm 0.05\text{mm}$
3. The pad layout is for reference purposes only

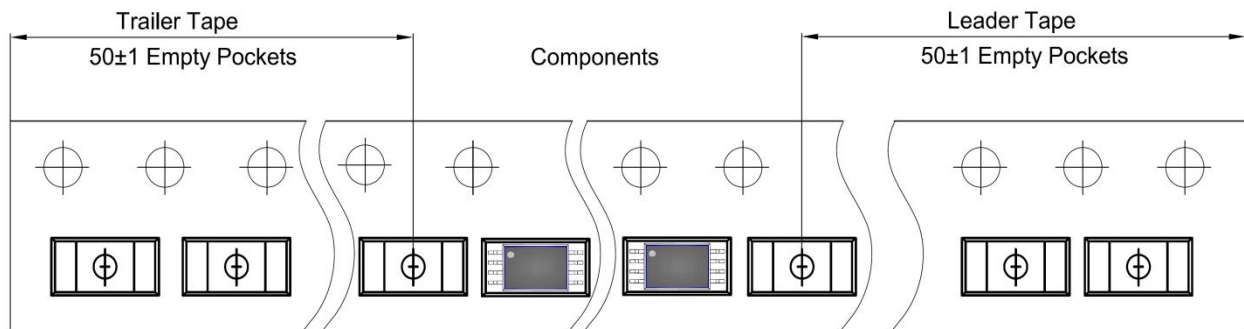
DUAL P-CHANNEL ENHANCEMENT MODE FET

TSSOP-8 Tape and Reel

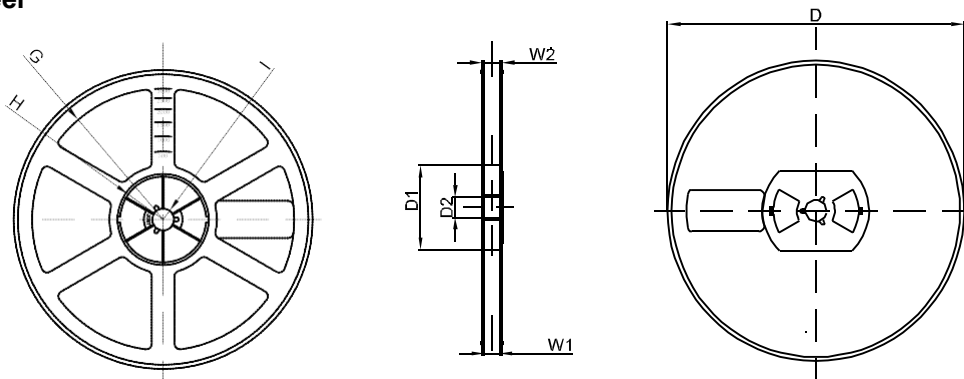
TSSOP-8 Embossed Carrier Tape

[illegible]

TSSOP-8 Tape Leader and Trailer



TSSOP-8 Reel



	DIMENSIONS ARE IN MILLIMETER							
REEL OPTION	D	D1	D2	G	H	I	W1	W2
13" DIA	Ø330.00	100.00	13.00	R151.00	R56.00	R6.50	12.40	17.60
TOLERANCE	±2	±1	±1	±1	±1	±1	±1	±1