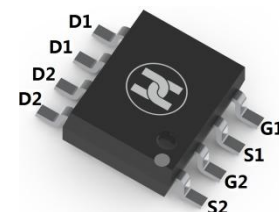
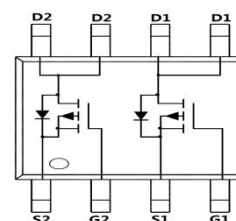


Dual P-Channel Enhancement Mode Field Effect Transistor
FEATURES

- Low on-resistance: $V_{DS}=-30V, I_D=-5A, R_{DS(ON)} \leq 49m\Omega @ V_{GS}=-10V$
- Low gate charge
- For load switch or in PWM applications.
- Surface Mount device


SOP-8

MECHANICAL DATA

- Case: SOP-8
- Case Material: Molded Plastic. UL flammability
- Classification Rating: 94V-0
- Weight: 0.3 grams (approximate)

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-source voltage		V _{DS}	-30	V
Gate-source voltage		V _{GS}	±12	V
Continuous drain current	T _A = 25°C	I _D	-5	A
	T _A = 70°C		-4.2	A
Pulsed drain current		I _{DM}	-30	A
Power dissipation	T _A = 25°C	P _D	2	W
	T _A = 70°C		1.44	W
Thermal resistance from Junction to ambient		R _{θJA}	110	°C/W
Thermal resistance from Junction to Lead		R _{θJL}	40	°C/W
Junction temperature		T _J	150	°C
Storage temperature		T _{STG}	-55 ~+150	°C

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Drain-Source breakdown voltage	$V_{(BR)DSS}^*$	-30			V	$V_{GS}=0V, I_D=-250\mu A$
Zero gate voltage drain current	I_{DSS}^*			-1	μA	$V_{DS}=-24V, V_{GS}=0V$
Gate-body leakage current	I_{GSS}^*			± 100	nA	$V_{DS}=0V, V_{GS}=\pm 12V$
Gate-threshold voltage	$V_{GS(th)}^*$	-0.7	-1	-1.3	V	$V_{DS}=V_{GS}, I_D=-250\mu A$
On-State Drain Current	$I_{D(ON)}$	-25			A	$V_{DS}=-5V, V_{GS}=-4.5V$
Drain-source on-resistance	$R_{DS(ON)}^*$		42.5	49	m Ω	$V_{GS}=-10V, I_D=-5A,$
				74	m Ω	$V_{GS}=-10V, I_D=-5A, T_J=125^\circ\text{C}$
			54	64	m Ω	$V_{GS}=-4.5V, I_D=-4A$
			80	120	m Ω	$V_{GS}=-2.5V, I_D=-1A$
Forward transconductance	g_{FS}	7	11		S	$V_{DS}=-5V, I_D=-5A$
Diode forward voltage	V_{SD}		-0.75	-1	V	$I_S=-1A, V_{GS}=0V$
Diode forward current	I_S			-3	A	
Input capacitance	C_{iss}		952		pF	$V_{DS}=-15V, V_{GS}=0V, f=1\text{MHz}$
Output capacitance	C_{oss}		103		pF	
Reverse transfer capacitance	C_{rss}		77		pF	
Gate resistance	R_g		5.9		Ω	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$
Total gate charge	Q_g		9.5		nC	$V_{GS}=-4.5V, V_{DS}=-15V, I_D=-5A$
Gate-source charge	Q_{gs}		2		nC	
Gate-drain charge	Q_{gd}		3.1		nC	
Turn-on delay time	$t_{d(on)}$		12		nS	$V_{GS}=-10V, V_{DS}=-15V,$ $R_{GEN}=6\Omega, R_L=3\Omega$
Turn-on rise time	t_r		4		nS	
Turn-off delay time	$t_{d(off)}$		37		nS	
Turn-off fall time	t_f		12		nS	
Body Diode Reverse Recovery Time	t_{rr}		21		nS	$I_F=-5A, dI/dt=100A/\mu s$
Body Diode Reverse Recovery Charge	Q_{rr}		13		nC	$I_F=-5A, dI/dt=100A/\mu s$

*Pulse test ; Pulse width =80 μs , Duty cycle $\leq 0.5\%$.

Dual P-Channel Enhancement Mode Field Effect Transistor

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

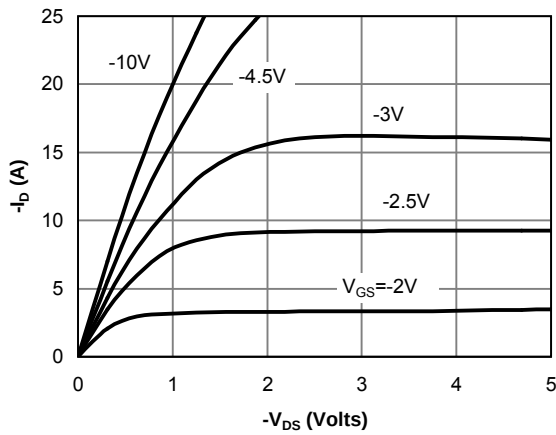


Fig 1: On-Region Characteristics

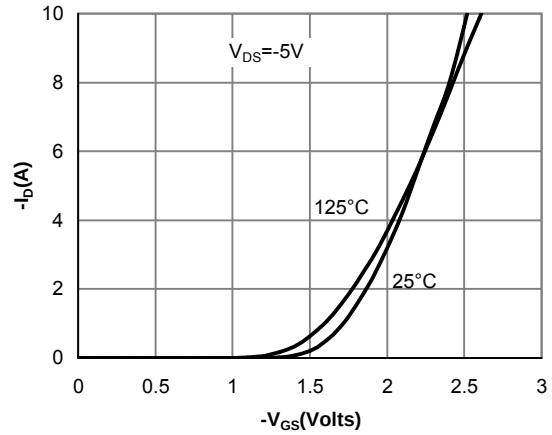


Figure 2: Transfer Characteristics

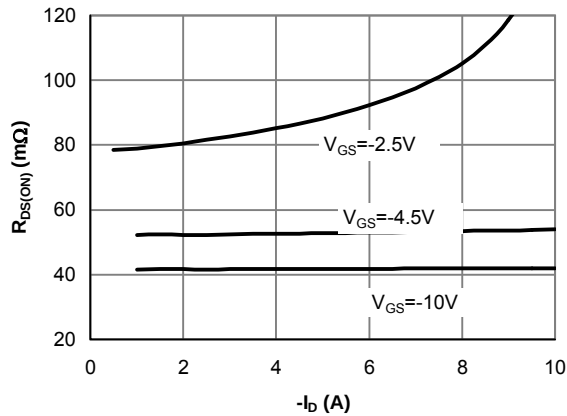


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

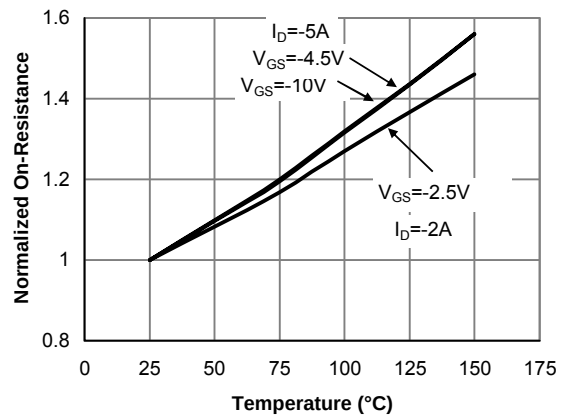


Figure 4: On-Resistance vs. Junction Temperature

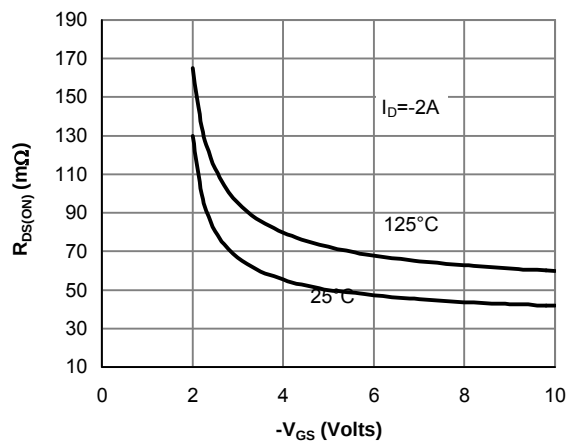


Figure 5: On-Resistance vs. Gate-Source Voltage

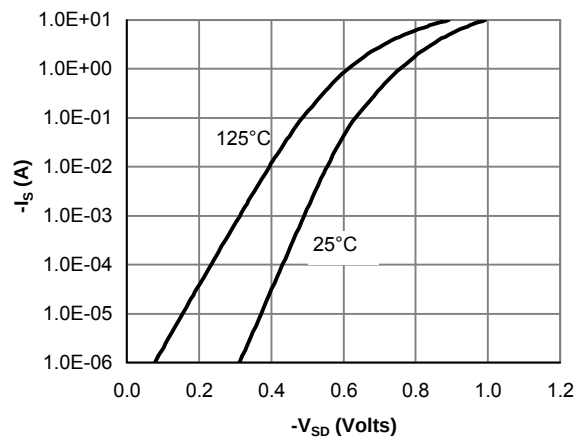


Figure 6: Body-Diode Characteristics

Dual P-Channel Enhancement Mode Field Effect Transistor

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

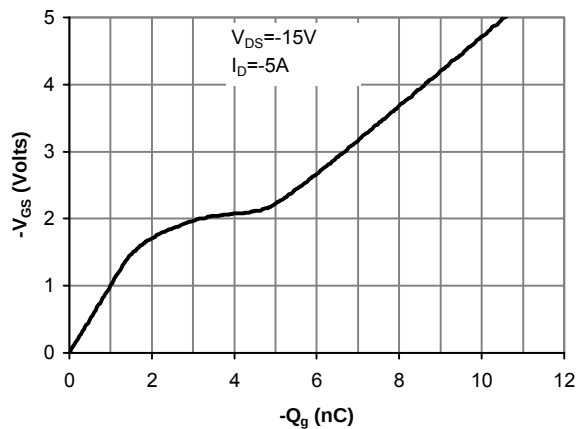


Figure 7: Gate-Charge Characteristics

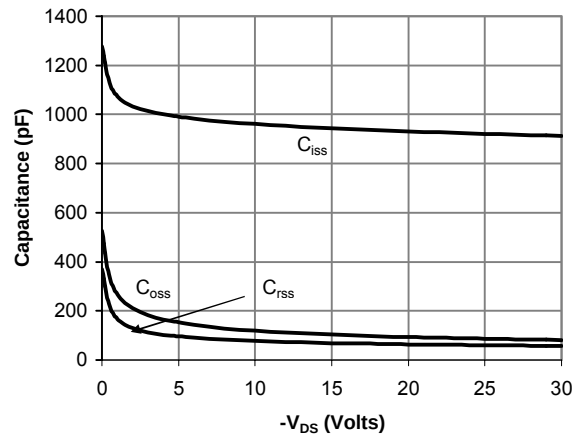


Figure 8: Capacitance Characteristics

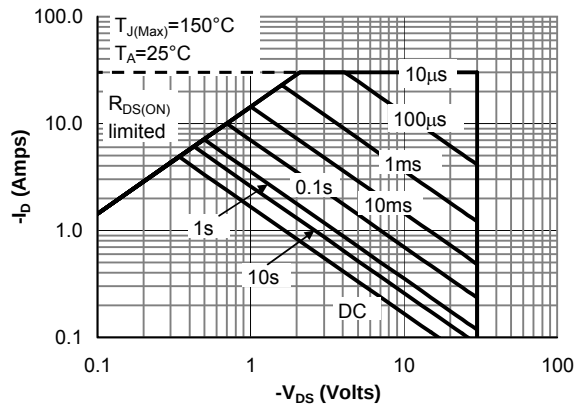


Figure 9: Maximum Forward Biased Safe Operating Area
(mounted on 1 in² FR-4 board)

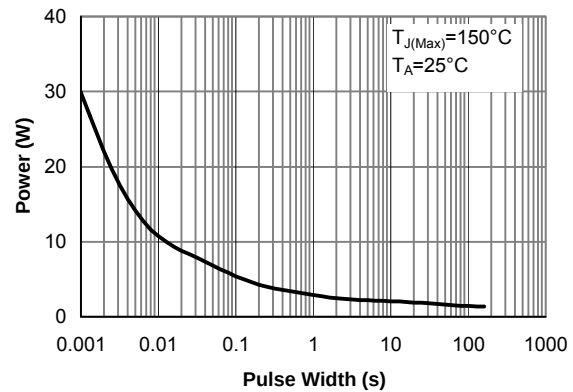


Figure 10: Single Pulse Power Rating Junction-to-Ambient
(mounted on 1 in² FR-4 board)

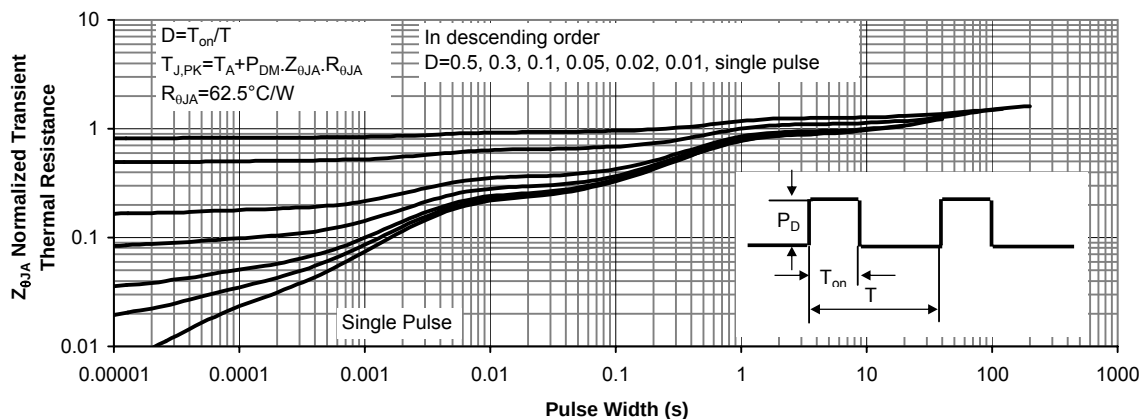
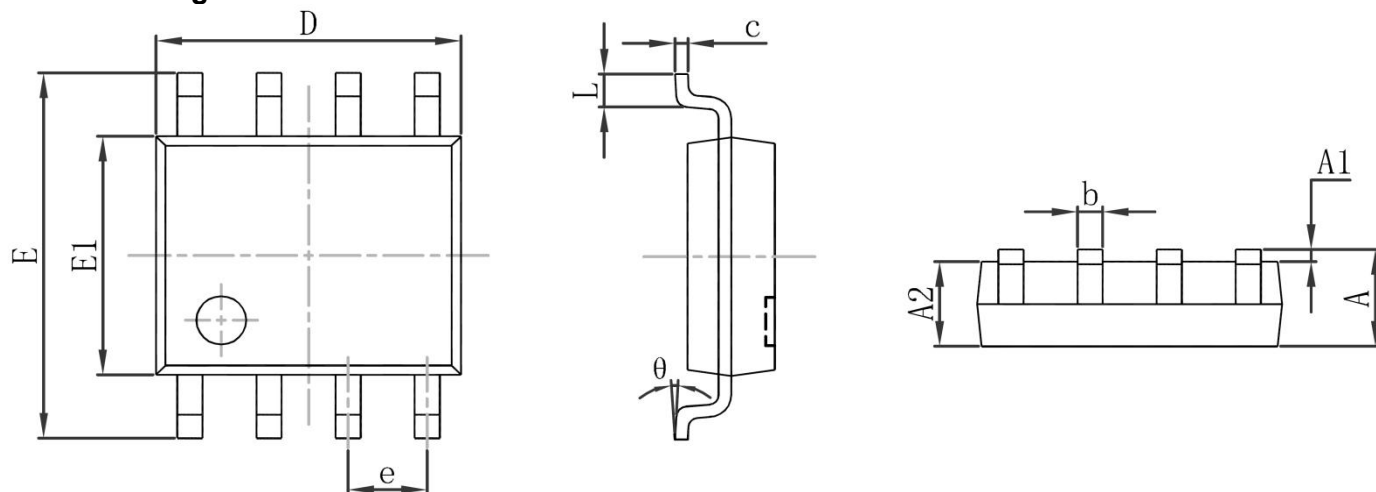
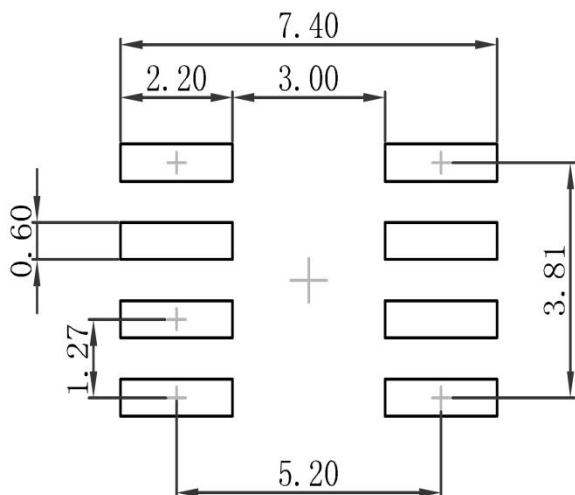


Figure 11: Normalized Maximum Transient Thermal Impedance

Dual P-Channel Enhancement Mode Field Effect Transistor
SOP-8 Package Outline Dimensions


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270(BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

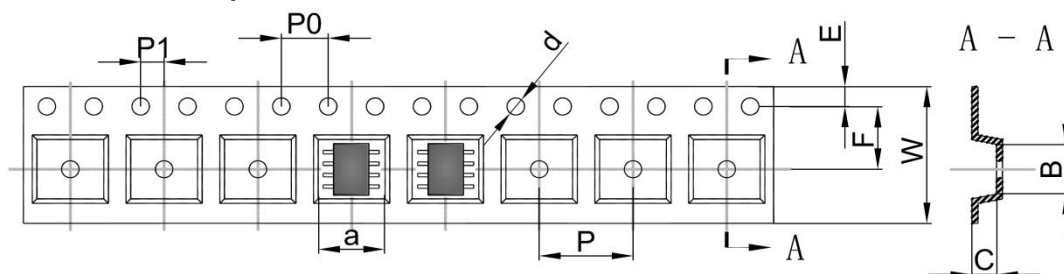
SOP-8 Suggested Pad Layout

Note:

1. Controlling dimension: in millimeters
2. General tolerance: $\pm 0.05\text{mm}$
3. The pad layout is for reference purposes only

Dual P-Channel Enhancement Mode Field Effect Transistor

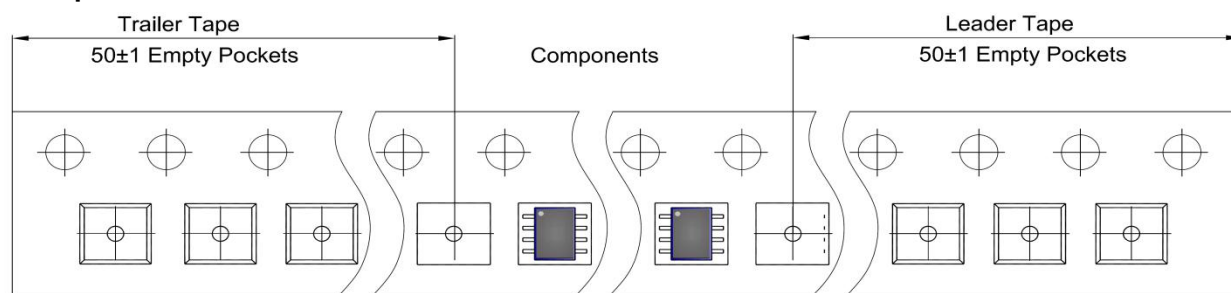
SOP-8 Tape and Reel

SOP-8 Embossed Carrier Tape

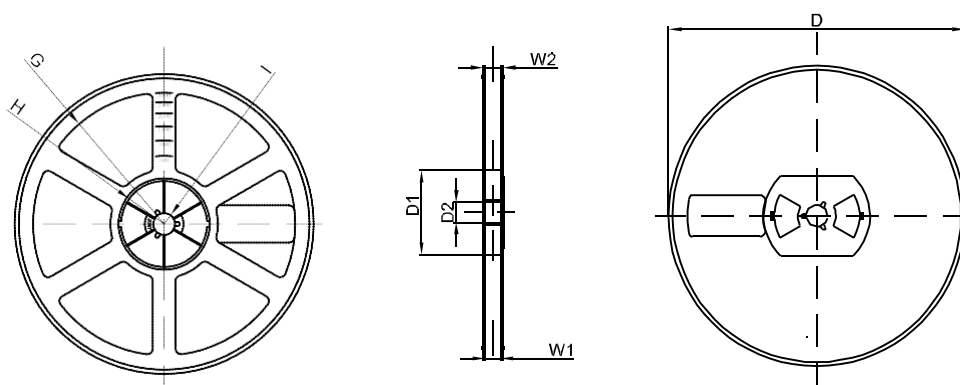


	DIMENSIONS ARE IN MILLIMETER									
TYPE	A	B	C	d	E	F	P0	P	P1	W
SOP-8	6.40	5.40	2.10	Ø1.50	1.75	5.50	4.00	8.00	2.00	12.00
TOLERANCE	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1

SOP-8 Tape Leader and Trailer



SOP-8 Reel



	DIMENSIONS ARE IN MILLIMETER							
REEL OPTION	D	D1	D2	G	H	I	W1	W2
13" DIA	Ø330.00	100.00	13.00	R151.00	R56.00	R6.50	12.40	17.60
TOLERANCE	±2	±1	±1	±1	±1	±1	±1	±1